CHARGE-COUPLED DEVICES FOR ANALOG-TO-DIGITAL CONVERSION

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Robert Carroll Michelson

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CHARGE-COUPLED DEVICES FOR

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Approved:

Joseph A. Connelly, Chairman

Harry A. Ecker

Thomas K. Gaylord

Dale C. Ray

Date approved by Chairman: 11/18/74

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Special permission was received from the Division of Graduate Studies to vary the form of the figure captions from that specified in the Thesis Manual, in order that this thesis be offered for publication in certain journals.

I dedicate this work to the glory of our Lord.

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INTRODUCTION

Current ECL and Schottky logic circuitry is capable of maximum switching frequencies in the order of 125 MHz [20]. Such rates would suggest that signal processing could be done at a comparable clock rate, which, in many cases, could lead to real-time data processing. However, present digital signal processing systems involving eight or more bits, are limited to processing rates of 10 to 20 MHz because the analog data cannot be converted to a digitally compatible form by the analog-to-digital (A/D) converter at a high enough rate. In most cases, the digital processor is capable of much greater speed. Therefore the A/D conversion of signal data is frequently the limiting factor in total system processing speed.

Recently Phillips Research Laboratories of the Netherlands operated charge-coupled devices (CCD) at frequencies in excess of 100 MHz with transfer efficiencies as high as 99.99 percent. Since these are merely prototype devices, it is projected that operation within the Gigahertz range will soon be possible using what is known as a 'peristaltic' charge-coupled device [6].

Even though CCD technology is still in its infancy, findings such as these indicate that charge-coupled devices could prove extremely promising when applied to the problems of A/D conversion. The purpose of this thesis research will be to produce an original design using charge-

coupled device technology as a means of achieving a fast analog-to-digital conversion scheme that is reliable, simple, and cost effective.

CHAPTER II

CCD OPERATION

Charge coupling, having been introduced in the late sixties, is a relatively new concept in metal-oxide semiconductor (MOS) technology. Charge coupling provides the basic functions of data storage and transfer of both digital and analog data [4]. In addition, charge-coupled devices feature the principal advantages of the presently existing MOS technology such as the basic fabrication steps, small surface area, and low power consumption. A comparision of CCD technology to bipolar and PMOS technologies is given for the case of an LSI encrypting system in Table 1 below.

Table 1. [19] Comparison of CCD Technology vs. Bipolar and PMOS Technologies in the Implementation of an LSI Encrypting System

Parameter	CCD LSI	Bipolar LSI	PMOS LSI
Number of LSI chips required to complete encrypting function	1	5	6
Size of LSI chips	80 x 80 mil^2	150 x 175 mil^2 each	150 x 150 mil^2 each
Total power for complete function (at max. clock rate)	0.02 watts	5 watts	2 watts
Types of Devices/ Logic circuits assumed	Standard two-phase over-lapping gate structure	Emitter logic	Standard three-phase dynamic logic

Figure 1a shows a schematic cross section of a single element charge-coupled device. CCD's operate by transferring quantities of charge between potential wells created in a doped semiconductor material just below the semiconductor-insulator interface. These potential wells are actually inversion layers formed in the semiconductor material. Figures 1b and c show how the inversion layer is formed in the P-type semiconductor material when a positive voltage is applied to the electrode. Since the electrode is electrically insulated from the semiconductor material, an electrostatic field is produced which repels majority carriers (holes) and attracts minority carriers (electrons).

Input Techniques

Once an inversion layer has been established, charge can be injected into the potential well by any method that is capable of creating minority carriers. Three popular methods for entering charge are shown in Figure 2. Figure 2a shows charge injection where a sufficiently large positive voltage is applied to the electrode to induce avalanche breakdown in the semiconductor material. During the avalanche breakdown, electrons are literally ripped from the outer shells of the substrate atoms nearest the semiconductor-insulator interface where the electrostatic fields are most intense. These liberated electrons then are held within the potential well created by the positive voltage on the electrode, and constitute an input to that well.

The most versatile method of entering charge is shown in Figure 2b. An N-region formed in the P-substrate will act as a source of minority carriers. Applying a bias as shown to the resulting P-N

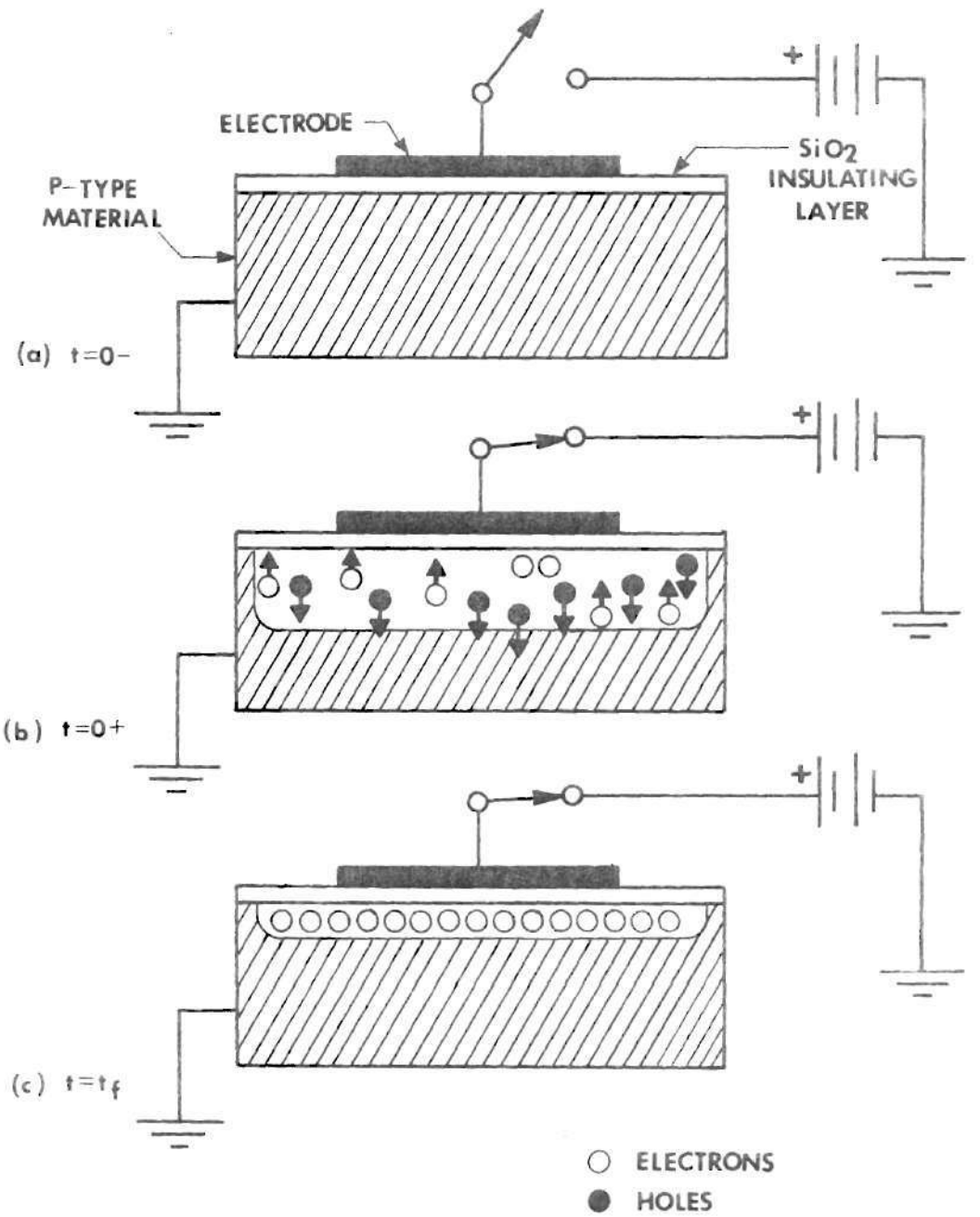

FIGURE 1

INVERSION LAYER FORMATION IN A SINGLE CCD ELEMENT [1]

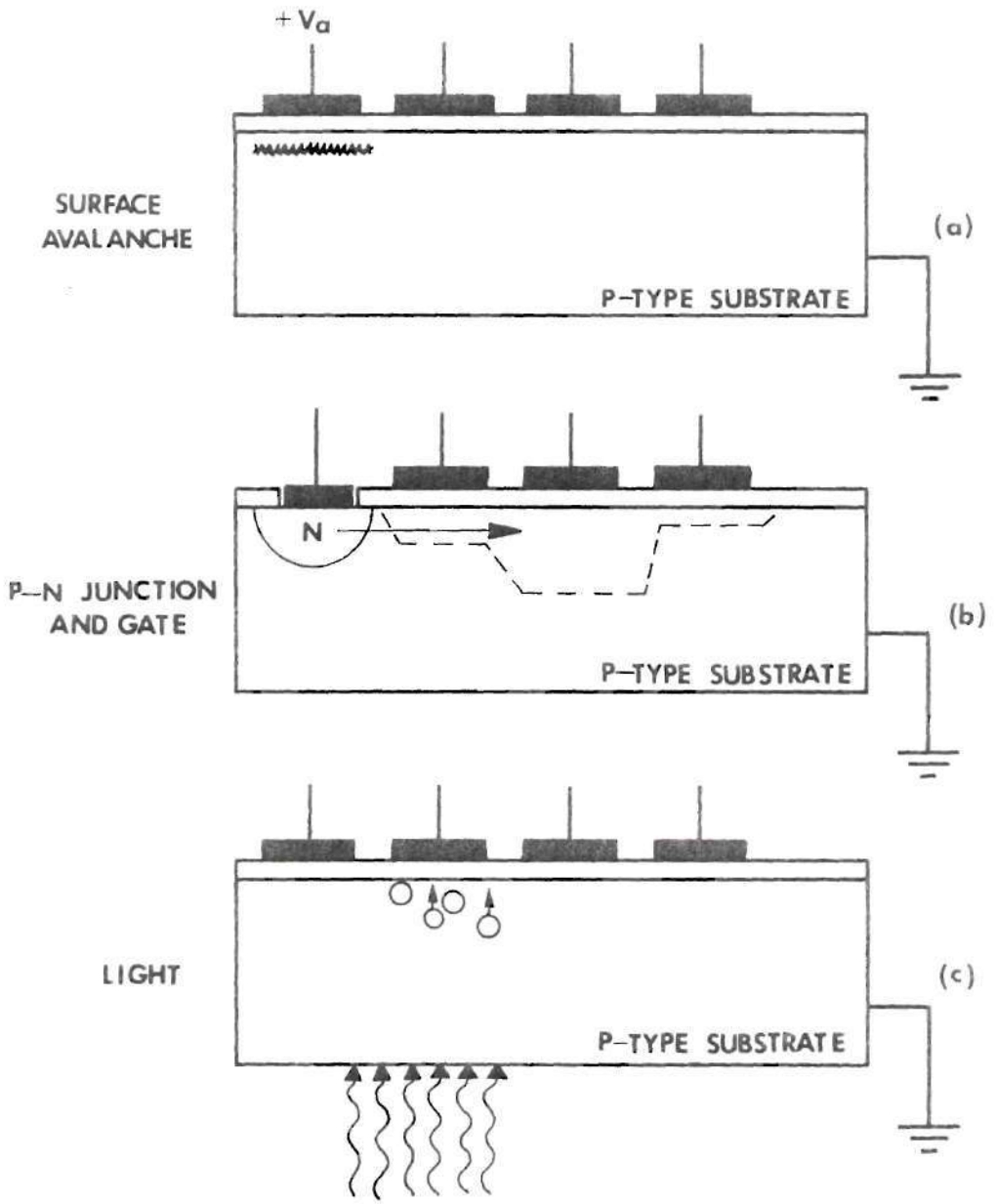

FIGURE 2

INPUT TECHNIQUES

junction while an inversion region is present nearby, will result in conduction of minority carriers from the N-region to the potential well. These quantities of charge that accumulate within the potential wells are referred to as 'packets', and can be used to represent either analog or digital information.

Figure 2c shows how minority carriers can be generated within the semiconductor by exposing it to localized electromagnetic radiation (especially that falling within the visible range). Those minority carriers generated within a diffusion length of the potential well will accumulate in the well in proportion to the photon density.

Charge Transfer

When several elements are placed in a row on a common substrate, a charge packet in the first potential well can be made to propagate sequentially from well to well. In general, a two-phase clock can be used to achieve unidirectional movement; however, if a three-phase clock is used, bidirectional movement is possible. Figures 3 and 4 show how both three- and two-phased clocking schemes operate by making an analogy between charge flow and liquid flow. According to Amelio [1], "the machine illustrated consists of a repeating series of three reciprocating pistons with a crankshaft and connecting rods to drive them. On top of one or more of the pistons is a fluid. Rotating the crankshaft in a clockwise manner causes the fluid to move to the right. If the crankshaft were to be rotated in a counter-clockwise manner, on the other hand, the fluid would move to the left." This particular type of arrangement, which requires three pistons to repeat the pattern, is a three-

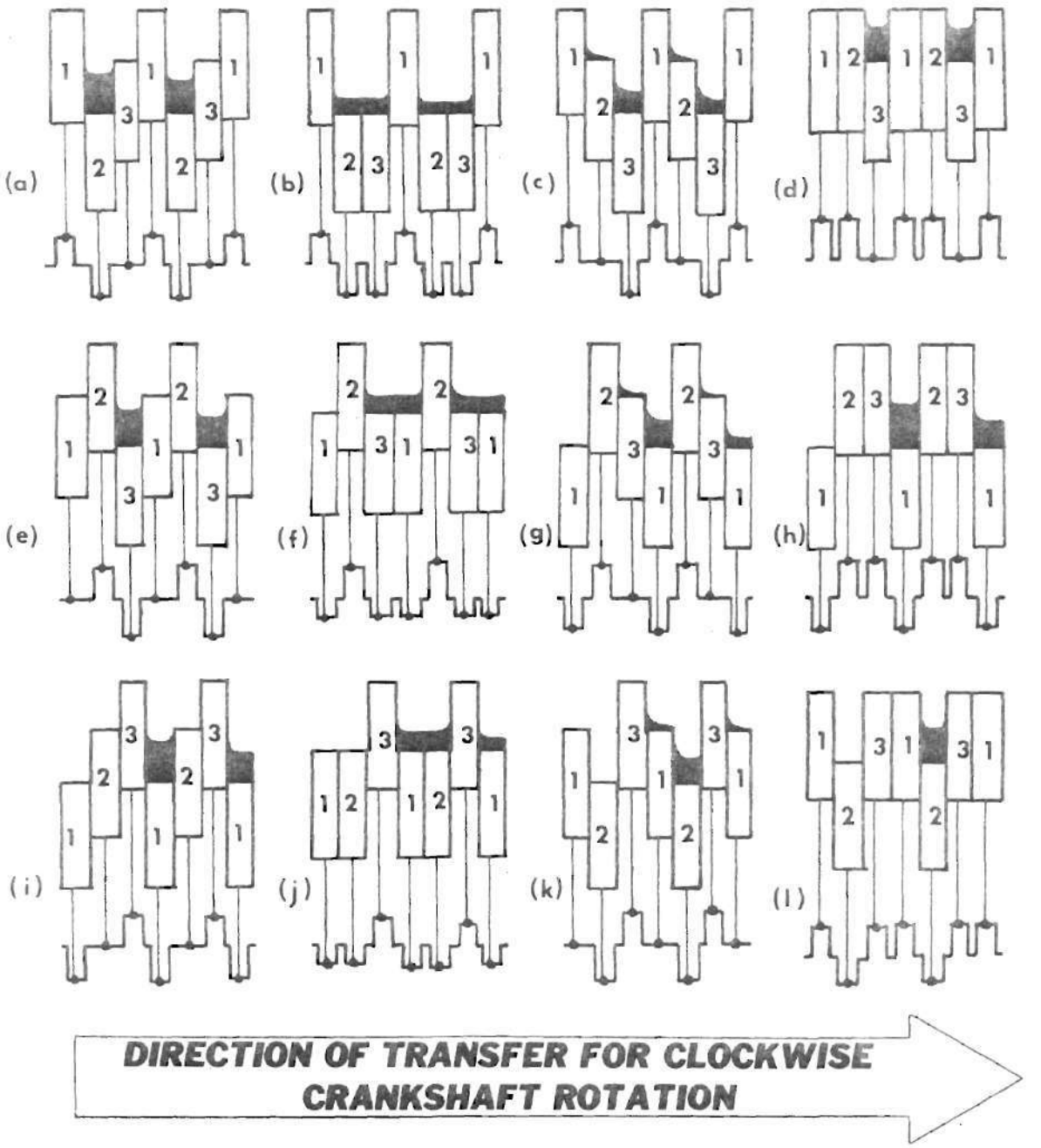

FIGURE 3

THREE-PHASE TRANSFER ANALOGY [1]

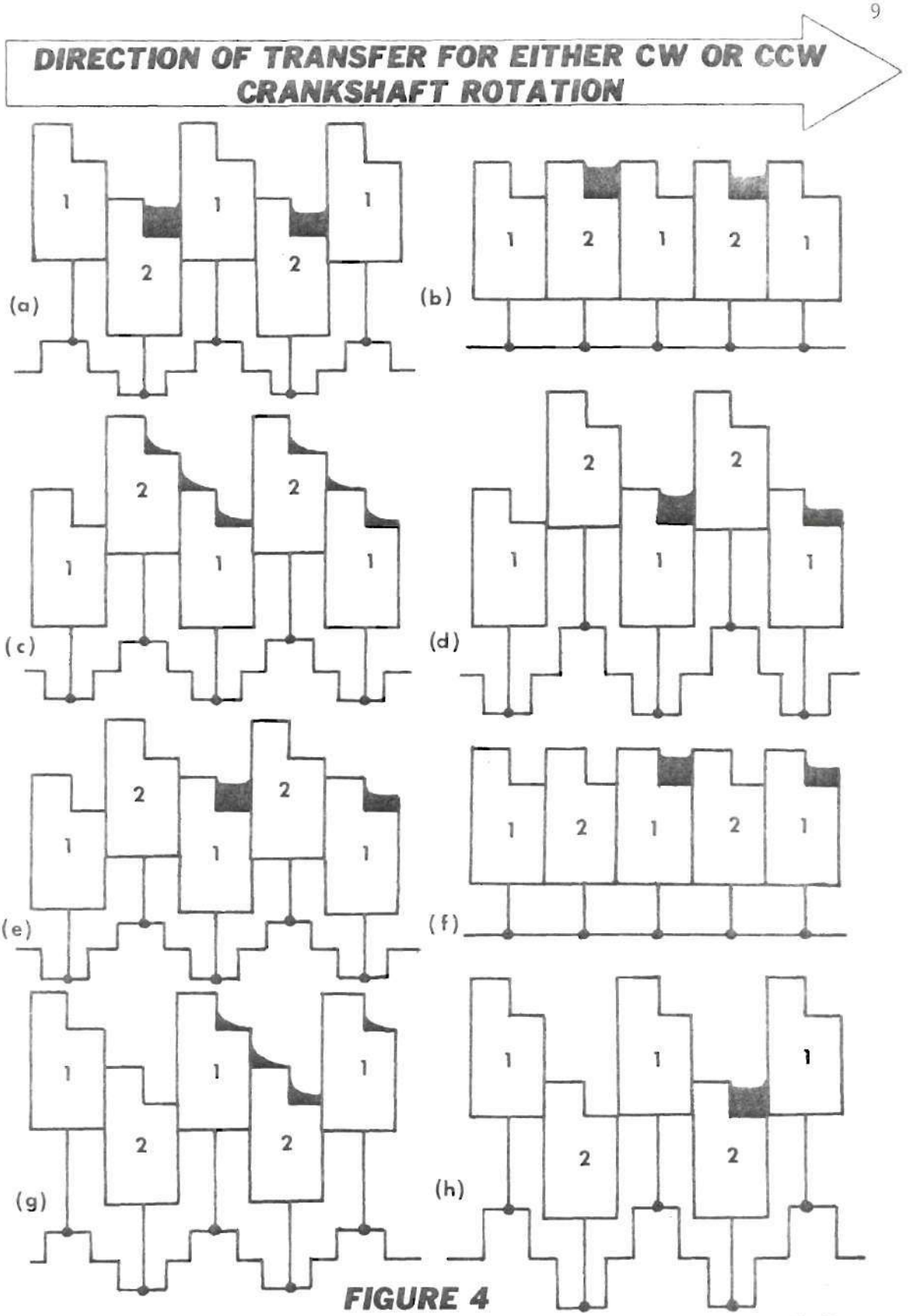

FIGURE 4

TWO-PHASE TRANSFER ANALOGY [1]

phase system. "Asymmetrical pistons are added to the mechanical analog in order to introduce the operating principle of a two-phase system. Regardless of the direction in which the crankshaft is rotated, the fluid now advances to the right. In the correspondence with an actual charge-coupled device the fluid represents an accumulation of electrons, the pistons represent the potential energy associated with the applied voltages and the crankshaft and the connecting rods represent the driving voltages and their timing" [1]. Figures 5 and 6 show actual three- and two-phase CCD systems along with the associated timing diagrams.

In the mechanical analogy of Figure 4, the asymmetrical piston heads make unidirectional flow possible with only a two-phase clock. In actual two-phase CCD systems, several methods can be used to add asymmetry to the inversion layer (where the inversion layer is analogous to the piston heads) thereby allowing the use of a two-phase clock. The most obvious of these is to shape the clock pulses asymmetrically. Another method is to make certain portions of each electrode physically closer to the substrate thereby causing the fields in these areas to be more intense. This results in localized increases in inversion layer depths. The method shown in Figure 6 uses diffused N-type islands located just under the insulating layer, that are offset from the electrode placement. These N-type islands cause the inversion layer to vary in depth with the proper asymmetry necessary for two-phase clocking.

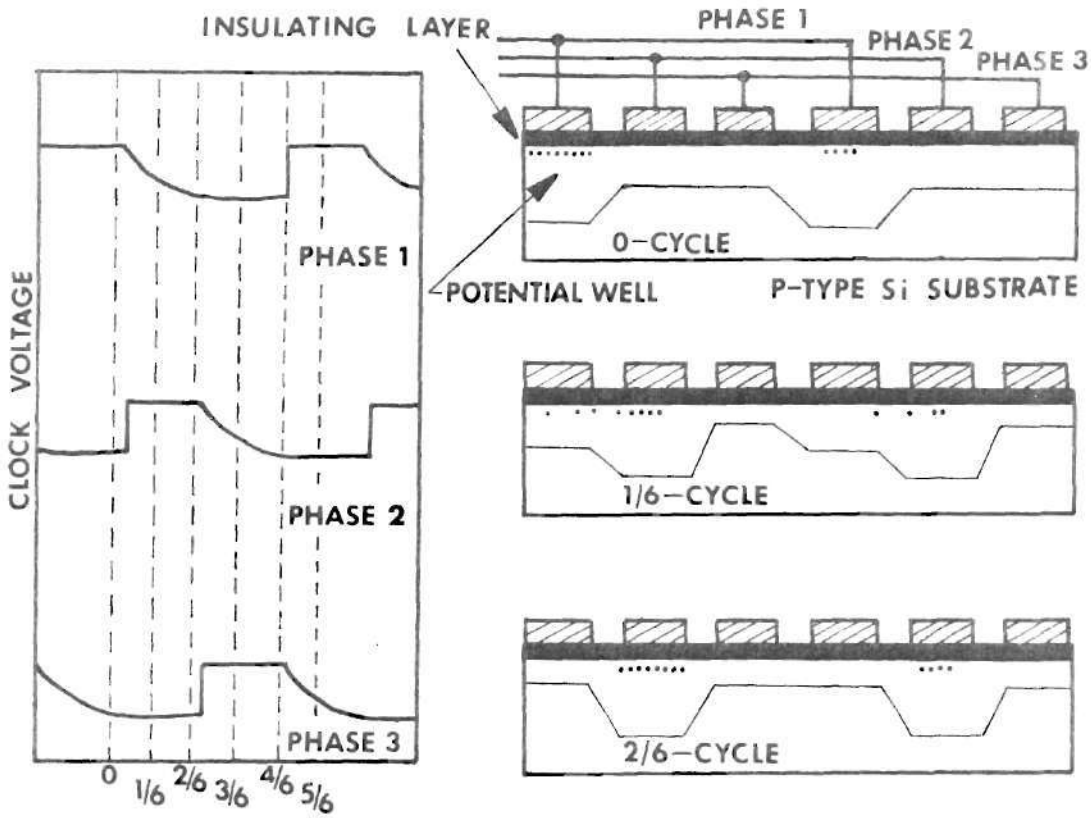

FIGURE 5

THREE-PHASE CCD SYSTEM AND TIMING

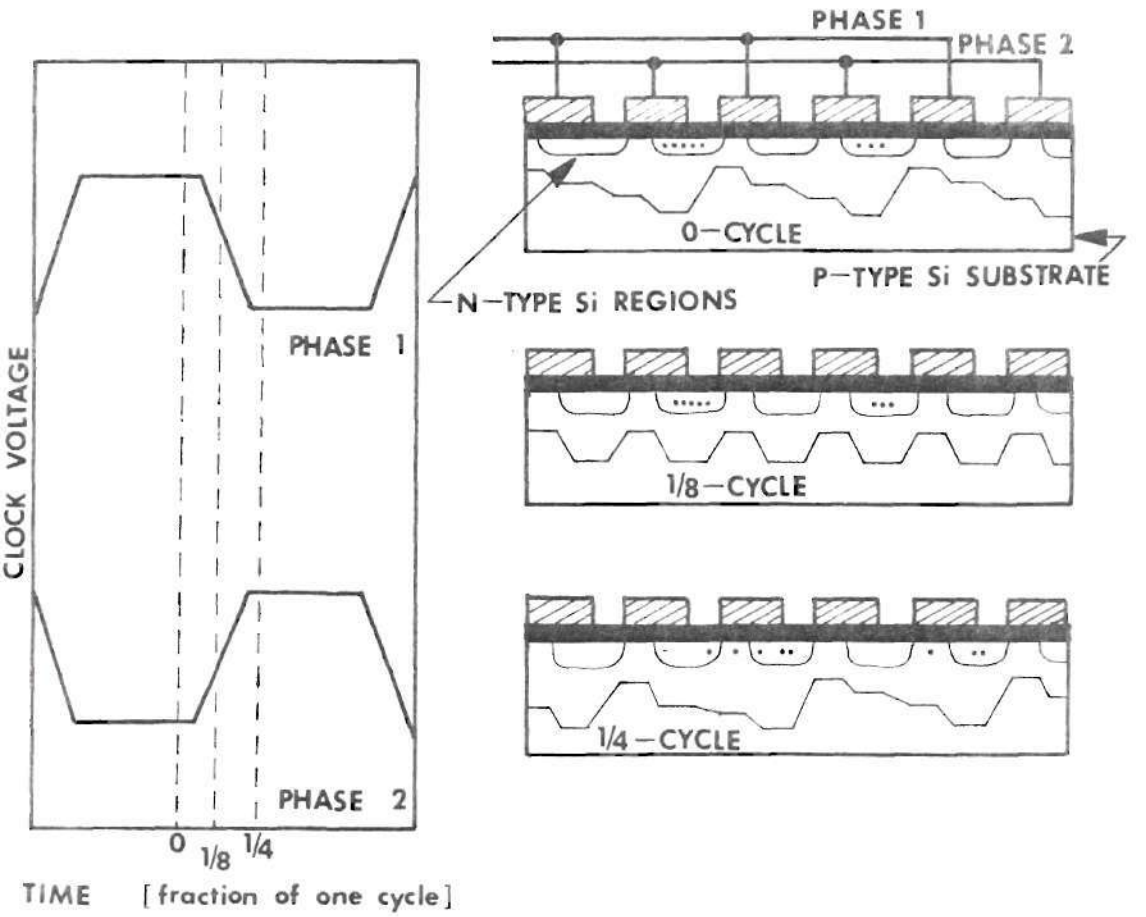

FIGURE 6

TWO-PHASE CCD SYSTEM AND TIMING

Output Techniques

Three common techniques exist for determination of the level of charge in a potential well. One technique which utilizes a floating gate amplifier (FGA), has the advantage that the charge density in a potential well can be detected without disturbing the charge. The FGA is essentially an MOS transistor with a gate that is insulated from the CCD channel current by the same SiO_2 layer that separates the transfer electrodes from the substrate. The FGA is therefore capacitively coupled to the well and senses charge without disturbing it.

A second technique for charge detection in a potential well is to create an N-region in the P-type substrate thus forming a P-N junction, or diode. Charge packets transferred into this output diode appear as output currents. This method is particularly useful at the end of shift registers where charge transfer is terminated. When an output diode is used, not only is the charge detected, but it is eliminated.

Charge injection is a third technique for detecting the amount of charge residing within a potential well. When a certain CCD element is to be interrogated by means of charge injection, the surface electrode above the element of interest is brought to the same potential as (or negative to) the P-type substrate. This causes the minority carriers to become free to diffuse into the substrate. (In the case of the negative electrode potential, the minority carriers are actually repelled out into the substrate). The amount of charge that was present in the well is then sensed by measuring the change in substrate potential. This technique can be of advantage when all of the CCD elements are to

be interrogated simultaneously as is the case in many imager schemes. However when only a few elements are to be interrogated, the liberated minority carriers will tend to be attracted to neighboring inversion layers that are still active. This disrupts the information stored within these areas and produces an erroneously low output reading due to the capture of minority carriers by neighboring elements.

CHAPTER III

A/D CONVERSION TECHNIQUES

To understand how charge-coupling could be used in the implementation of an analog-to-digital conversion system, consider the operation of three popular high-speed A/D conversion schemes that are representative of most non CCD systems in use today.

In the parallel or simultaneous (Flash) method, all n-bits of the digital word resulting from a conversion are determined simultaneously. A characteristic of this conversion scheme is that to convert n bits of binary information, $2^n - 1$ comparators are needed. Each comparator determines one LSB level [3]. Figure 7 shows a 3-bit A/D system employing the parallel method where each comparator has a different threshold. The threshold voltage of each comparator is derived from its position along a resistive ladder. The resistive ladder is a voltage divider with elements chosen to give weighted reference voltage outputs to the comparators. A binary weighting is shown in Figure 7, where the threshold voltages differ by powers of 2. Only those comparators whose threshold voltages are less than V_{in} will change state when an analog voltage is applied. Examination of all comparator outputs simultaneously simulates a 'thermometer-type' action; that is, the comparators change state in response to a change in analog input voltage in a way analogous to the mercury rising and falling in a thermometer. Referring to Figure 8, the lower comparators change state in response to a low input voltage, and as the voltage rises, more of the higher threshold comparators change

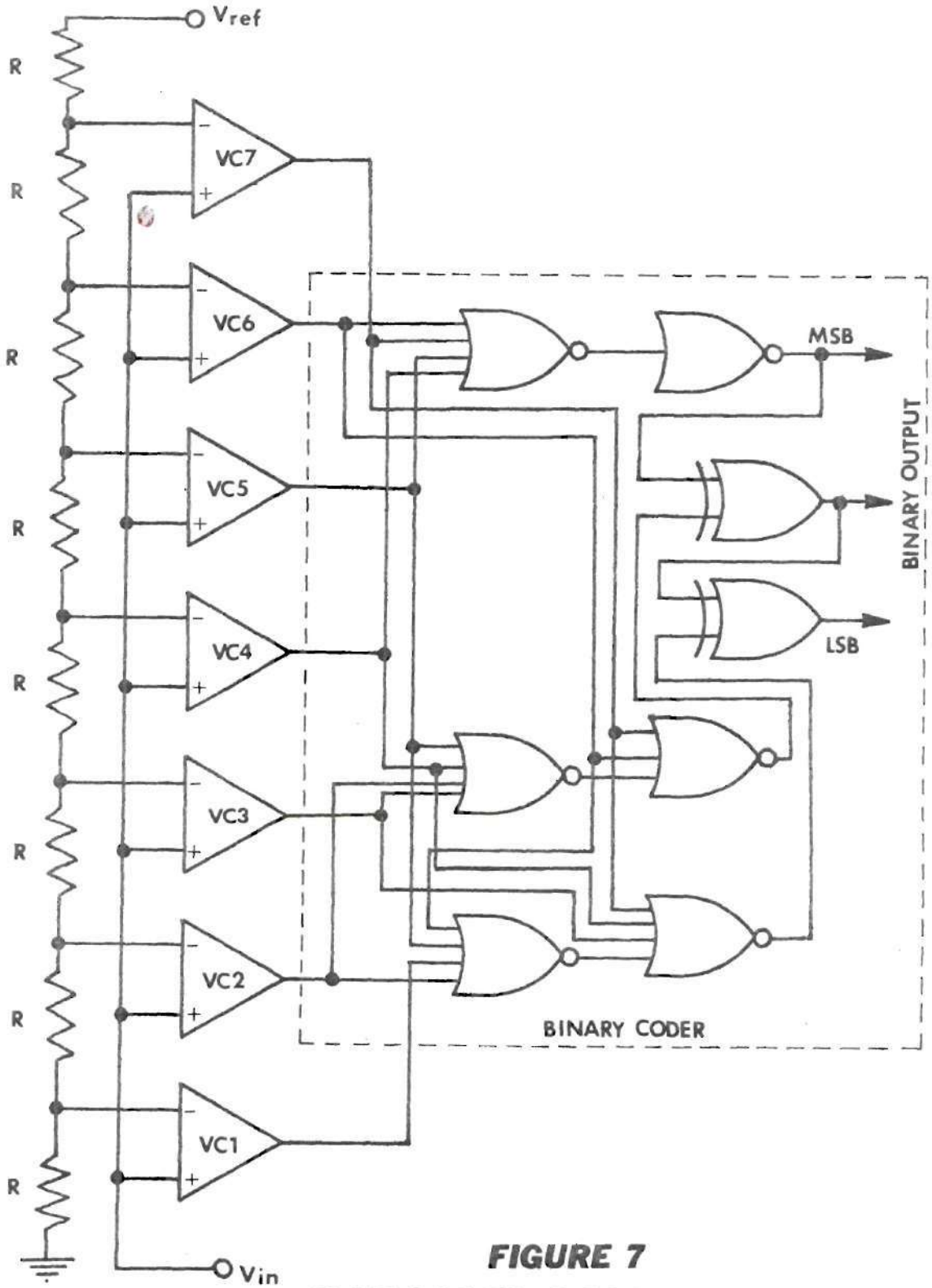

FIGURE 7

PARALLEL CONVERSION

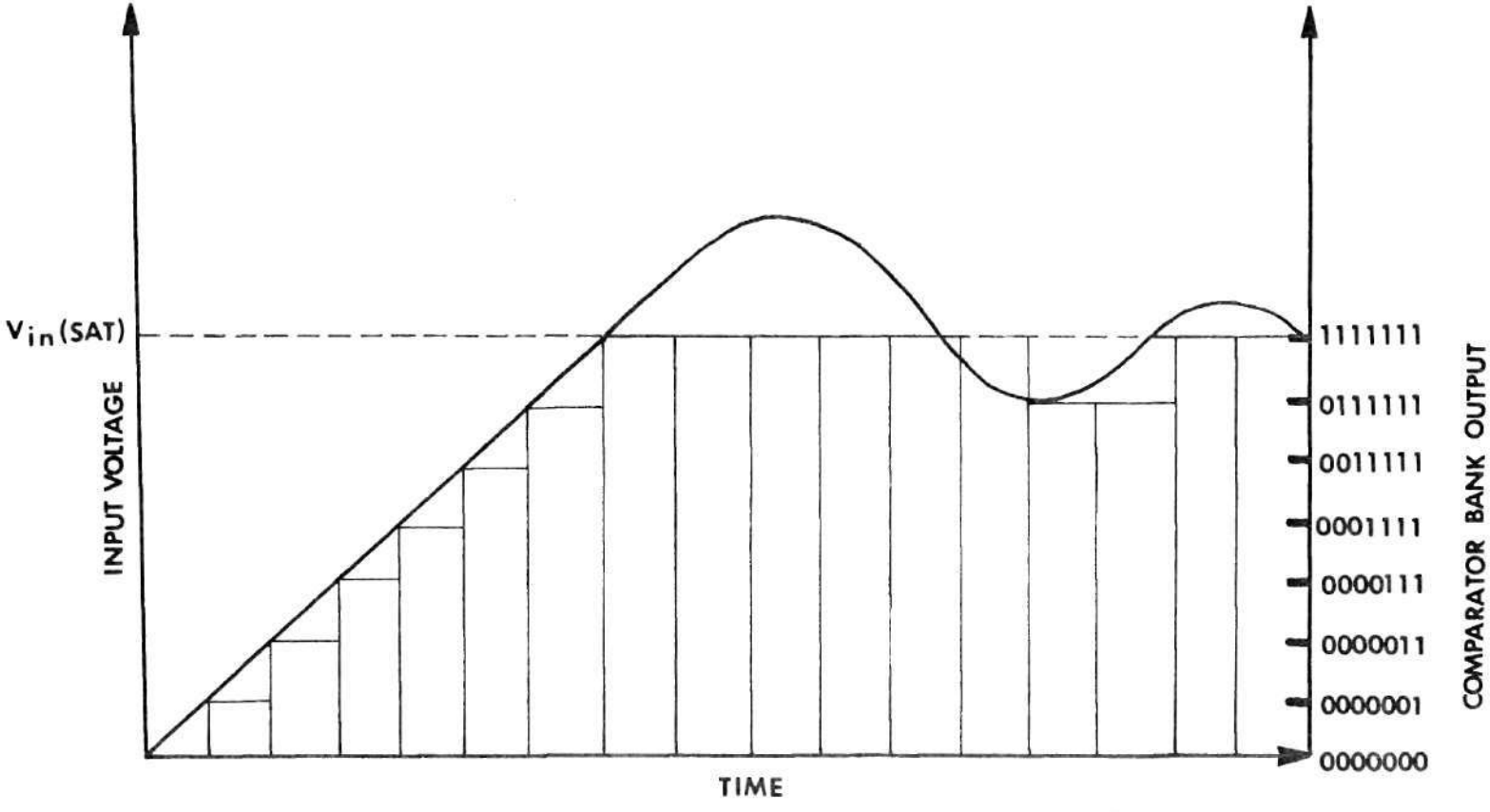

FIGURE 8

COMPARATOR BANK RESPONSE TO A VARYING INPUT FOR A 3-BIT PARALLEL CONVERTER

state until the string of comparators 'saturates' for further increase in V_{in}. This saturation simply refers to the fact that all of the comparators have changed state and there can be no further response to an increase in V_{in}.

Consider positive logic where a logic 0 and a logic 1 are identified with a low and high comparator output voltage, respectively. The outputs of the comparators, when considered simultaneously, form an n-bit binary word that has leading 0's and trailing 1's where the trailing 1's are the lower threshold comparator outputs. An example of the comparator bank output for an n-bit converter might appear as 000000 ... 00111111. The exception to the leading−0, trailing−1 pattern occurs when the output is saturated (i.e., all 1's) or when $V_{in} = 0$ thus yielding all 0 outputs.

Clearly the output word in the comparator bank is not in one of the commonly used binary codes (e.g., straight binary, BCD, Gray, etc.). Therefore decoding must be used. In general combinational logic is used for this decoding; however, a read-only memory (ROM) could be used as well. The use of a ROM is wasteful, though, because only a fraction of the possible input combinations are ever used and there is no way to use the multitude of 'don't care' conditions to reduce the overall circuit complexity. In Figure 7, combinational logic has been used to decode the comparator bank output to give a three-bit straight binary output.

The conversion time for a parallel A/D system is given by

$$T_c = t_c + kt_L \tag{1}$$

where t_c is the response time of a comparator, t_L is the propagation delay time of one level of combinational logic, and k is the number levels of logic in the decoder. Since comparators are available with nominal response times in the order of 30 ns, and propagation delays in combinational logic can be held to about 3 ns per logic level [20], the principal advantage of a parallel converter is short conversion time. In general, parallel converters will yield the shortest conversion times [17]. The major disadvantage is the complexity and number of components necessary for the system. The extent of decoding logic becomes massive when more than about six binary bits are desired as an output since a 6-bit decoder would have to decode $2^n - 1$, or 63 input lines down to six bits for a straight binary representation. The simple 7-input decoder used in Figure 7 requires 32 gate leads; a 63-input decoder would require several hundred. System complexity is even more apparent for an 8-bit converter because 255 comparators would be necessary thus requiring a 255-input decoder. In many cases this would prove prohibitive from both an economic standpoint and an engineering standpoint. Other A/D methods exist for reducing the component quantities with some corresponding increases in conversion time.

One such method is successive-approximation. This technique is capable of both high resolution (to 16 bits), and high speed (to 1 MHz throughput* rates). The speed of a successive-approximation converter is somewhat less than that of the parallel converter because of the serial nature of the system. As a minimum, one clock pulse is necessary for the conversion of each bit. Therefore, the higher the resolution, the longer

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*See Appendix I

the conversion time when assuming a fixed clock frequency. Therefore, it is desirable to have as high a clocking rate as possible without the clock period becoming less than the inherent response times and propagation delays of the elements comprising the converter. Figure 9 shows a block diagram representation of a successive-approximation converter. The minimum conversion time for such a circuit can be calculated from

$$T_{c(min)} = n[t_c + kt_L + t_{D/A} + t_{oa}] \tag{2}$$

where n is the number of output bits, t_c is the response time of the comparator to a voltage that just surpasses threshold, t_L is the propagation delay time of one level of combinational logic, k is the number of logic levels in the control logic $t_{D/A}$ is the propagation delay due to the digital-to-analog converter, and t_{oa} is the response time of the operational amplifier. Consequently, the maximum clocking frequency is

$$F_c = 1/[T_{c(min)}] \tag{3}$$

Referring to Figure 9, when the conversion command is applied, and the converter has been cleared (all outputs set to 0), the system begins the conversion procedure, by sequentially setting the bits of the storage register to logical 1's, starting with the most significant bit (MSB). As each bit is enabled, the comparator gives an output signifying that the input signal is greater or less in magnitude than the output of the digital-to-analog converter (D/A). If the D/A output is greater than the input signal, the bit is reset to a logic 0; otherwise the bit

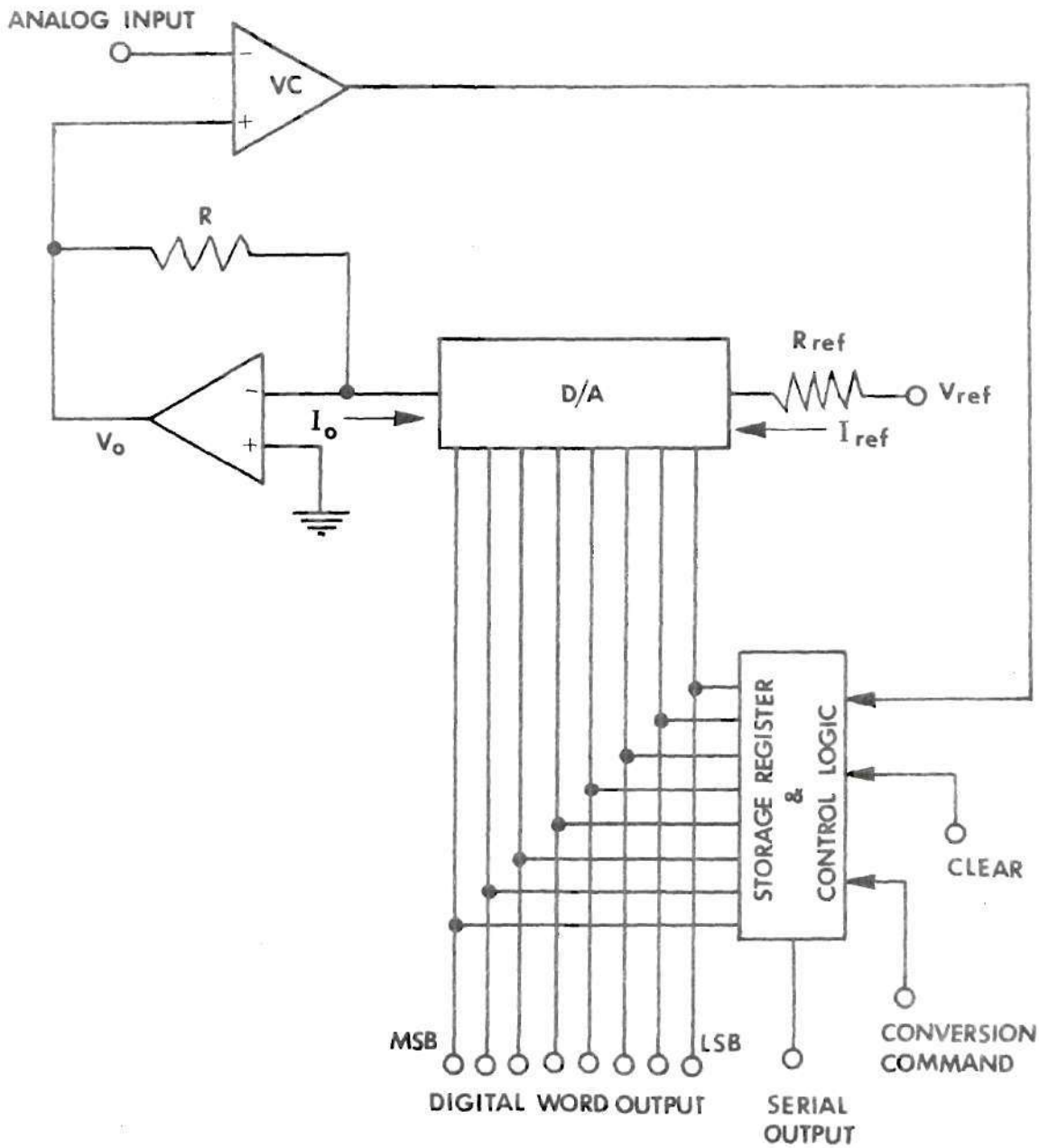


FIGURE 9

A/D SUCCESSIVE-APPROXIMATION [12]

remains a logic 1. The system does this with the MSB first, then the next most significant bit, then the next, etc. After all the bits of the storage register have been enabled and tested, the conversion cycle is complete and another conversion cycle may be initiated, Due to the sequential nature of this technique, successive approximation produces longer conversion times than the parallel conversion method; however, system complexity is decreased and system operational features usually compensate for the increased conversion time. Successive approximation systems feature a conversion time that is fixed and independent of the magnitude of the input voltage. Also, each conversion is unique and independent of the results of previous conversions because the internal logic is cleared at the start of each conversion [3]. Successive-approximation is, by far, the most widely use A/D system today [12].

The third, and perhaps the easiest and least complicated high-speed A/D scheme is the incremental converter. This technique utilizes a simple binary counter whose output serves as both the input for a D/A converter and as the final digital output (see Figure 10). After signals to clear previous data and to begin the conversion process are applied, the counter begins counting at the clock frequency. As the count increases, the analog output of the D/A converter likewise increases until it just exceeds the magnitude of the analog input to the comparator. At this time instant, the comparator changes state, inhibiting the clockline to the counter causing the count to stop. This final count is then a binary representation of the analog input signal. Note that unlike the parallel and successive-approximation techniques, the conversion time is dependent

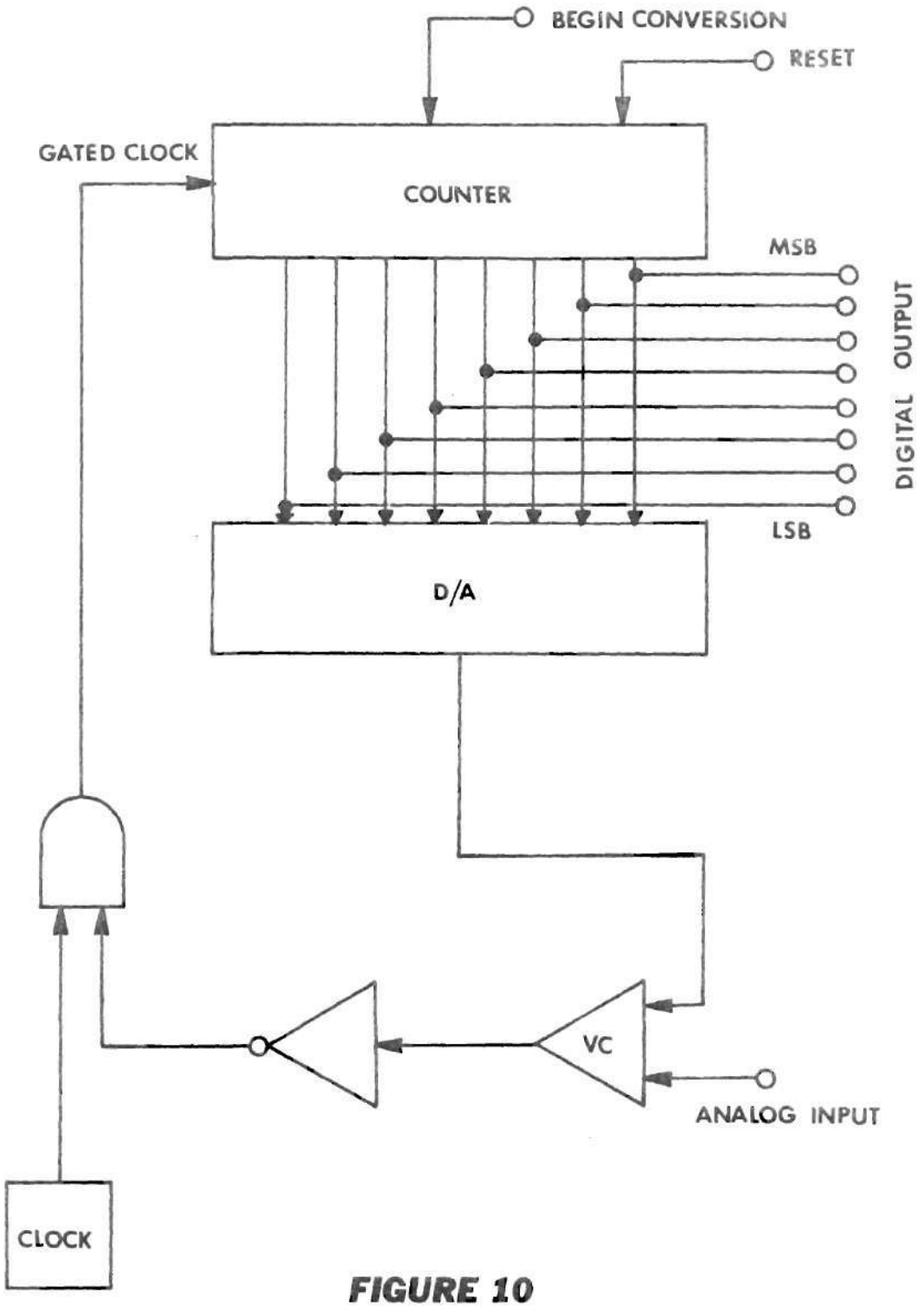


FIGURE 10

INCREMENTAL CONVERTER

on the magnitude of the analog voltage to be converted. Shorter conversion times occur for small analog voltages; here the conversion time approximates that of the parallel technique in that the counter may only have to count several pulses before the corresponding D/A output surpasses the analog input. For a large input voltage the counter may have to count nearly to the point of saturation before the D/A output can surpass the analog input. Therefore, the conversion time is equal to:

$$T_c = N/F_c + t_c + kt_L + t_{D/A} \tag{4}$$

where N is the number of clock pulses necessary for the count to exceed threshold and F_c is the clock frequency. The incremental conversion method has several drawbacks. As stated above, the conversion time depends on the magnitude of the analog input voltage. Also if the delays incurred in switching the comparator and signal propogation through the associated combinational logic are appreciable, the count sequence may exceed the actual representation of the analog input voltage before finally being inhibited. These time delays must be minimized when using this technique.

In summary, the parallel conversion technique results in the shortest conversion time; however its major limitation is the large number of components necessary for higher resolutions. The successive-approximation technique, on the other hand, requires fewer total components. However being a sequential method, this technique operates with longer conversion times than those achieved with a parallel system. The incremental conversion technique is the simplest approach, but only

achieves short conversion times when the analog input level is consistantly of low magnitude (or high magnitude, if the counter is made to count down instead of up).

In subsequent sections, CCD A/D techniques will be explored with the intent of bringing CCD technology together with A/D technology to produce a CCD-A/D system that is simple, reliable, and cost effective.

VTF - A Hybrid Approach

A flash converter requiring no decoding logic may be designed by modifying the parallel conversion technique with the addition of feedback. Such a system is known as a Variable Threshold Flash A/D converter or VTF. In its simplest form, a VTF is a non-synchronous, clockless A/D producing a binary coded output without requiring decoding logic. In addition, since feedback is used, the number of comparators required for an n-bit system is reduced from the $2^n - 1$ needed in a regular parallel conversion scheme, to just n.

Figure 11 shows a block diagram of a 3-bit VTF. The VTF is a hybrid cross between the parallel and successive-approximation converters mentioned earlier. It has the advantages of high-speed operation due to its parallel properties plus the simplicity attainable only in a serial method such as successive-approximation.

Referring to Figure 11, the three comparators initially have their threshold voltages set at binary weightings of the reference voltage; that is the MSB threshold is 1/2 V_{ref} and the second MSB 1/4 V_{ref}, etc. This type of threshold weighting is identical to that of a parallel conversion scheme. However, with the VTF scheme, the comparator threshold

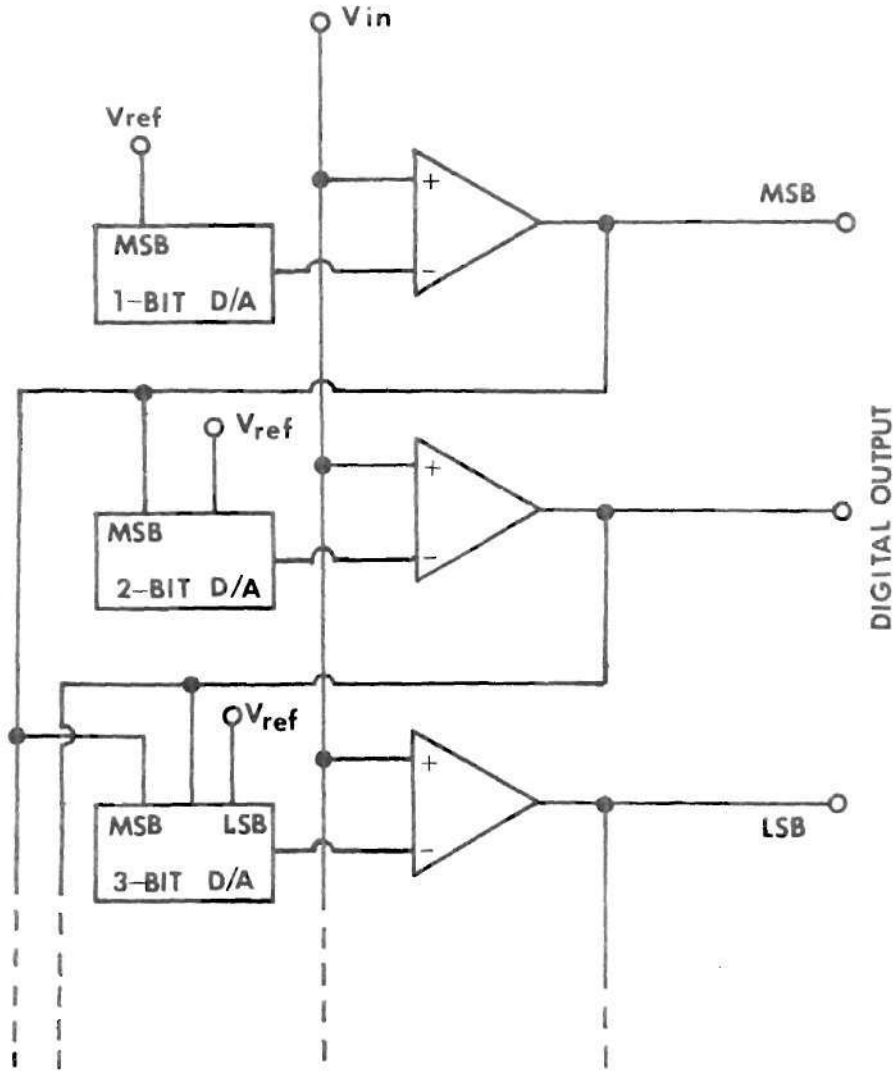


FIGURE 11

3-BIT VTF A/D WITH BINARY WEIGHTED OUTPUT [12]

voltages are changed during the conversion process so as to form the proper coded output from the converter. Note that a VTF system may therefore be set up to present outputs in not only binary, but BCD, Grey, or other codes by controlling the threshold voltage change.

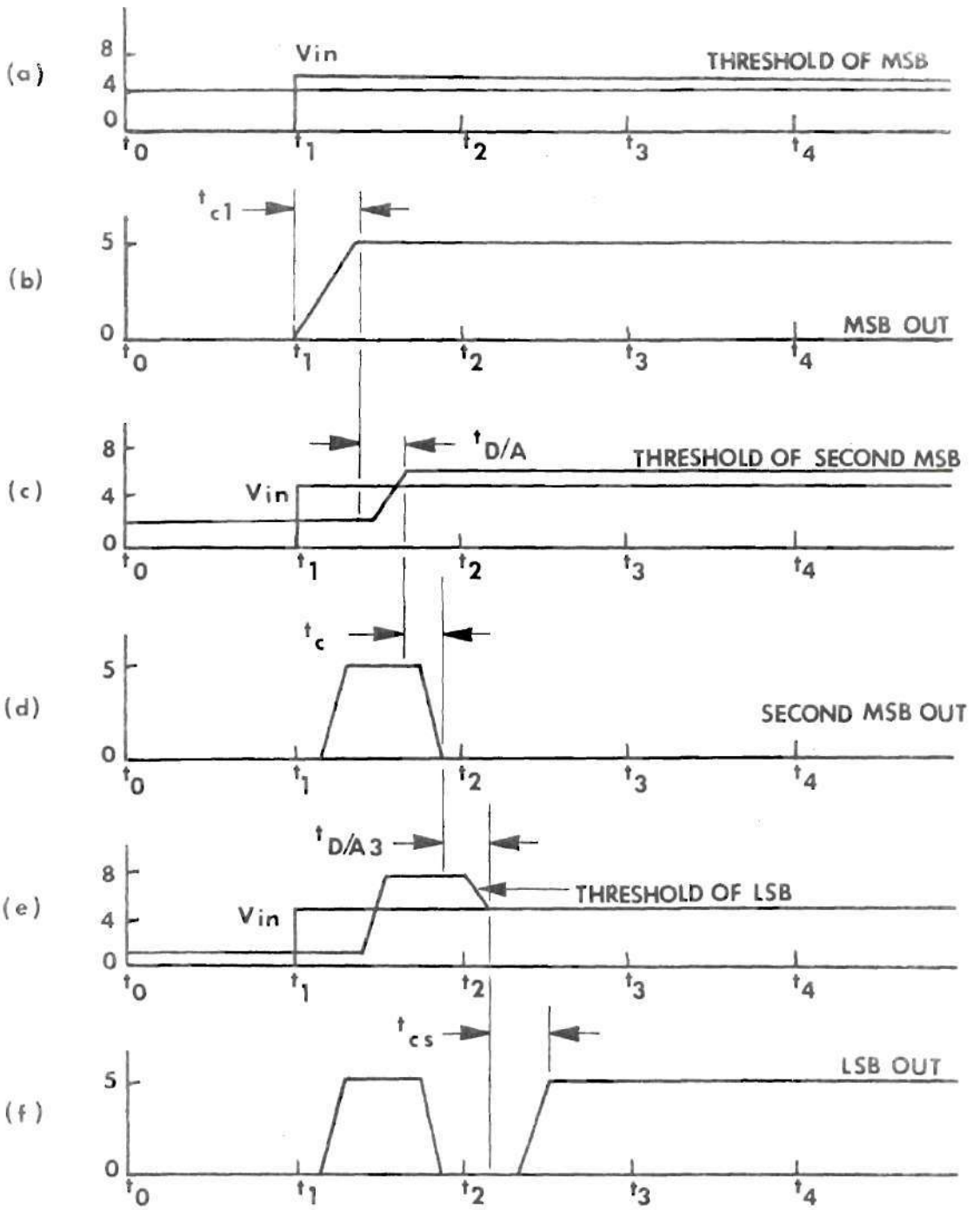
In Figure 11, the MSB uses a 1-bit D/A which produces a constant threshold voltage of 1/2 V_{ref} on the MSB comparator. The second most significant bit uses a D/A comprised of two bits. The LSB of this D/A produces a constant voltage of 1/4 V_{ref}. The other output of this second D/A is connected to the output of the MSB comparator resulting in the threshold of the NMSB comparator having two possible states; 1/4 V_{ref} and 3/4 V_{ref}.

The third MSB uses a 3-bit D/A where the LSB alone (i.e., the MSB and NMSB are equal to 0) produces a threshold voltage to the third MSB comparator of $V_{ref}/8$. The other two inputs of the D/A are used to produce three more possible states for the threshold voltage; $3V_{ref}/8$, $5V_{ref}/8$, and $7V_{ref}/8$.

Note that additional bits may be added as desired, without increasing the complexity of the preceding stages: for example, the MSB for the 3-bit converter shown in Figure 11 will be identical to that for an 8-bit system.

An example of the operation of a simple asynchronous VTF system is given in the literature by Henry [12] and is presented below.

> "As an example of how the system operates, let us assume that the circuit (in Figure 11) is in a steady condition with . . . zero volts on the input. The circuit is set up with a full scale of 8 volts. This gives the LSB a value of 1 volt. At time t_1 a step input is initiated of 5.1 volts. Figure 12 shows the waveforms of the system as it 'converts' the step input voltage to the digital word (101) output.



TOTAL TIME DELAY = $t_{c1} + t_{D/A_2} + t_{c_2} + t_{D/A_3} + t_{cs}$

$$V_{in} = \begin{cases} 0, & t_o \leq t < t_1 \\ 5.1, & t \geq t_1 \end{cases}$$

FIGURE 12

VTF WAVEFORMS [12]

For the purpose of this discussion, the propagation times of the comparators, t_c, are equal. Also, the settling times of the D/A's, $t_{D/A}$, are identical and equal to t_c.

Figure 12a shows the threshold of the MSB comparator and the input voltage, V_{in}. The output of the MSB is shown in Figure 12b." The remaining parts of this Figure show the same points for each of the other two bits respectively.

"From time t_0 to t_1 the input voltage to the system (V_{in}) is zero volts. The threshold of the comparators are at their lowest states, namely, 4, 2, and 1 volt respectively. As the input voltage is below all of the thresholds, the outputs of the comparators are all low."

At time t_1, a step input voltage of 5.1 volts is applied. "The input being greater than each of the respective threshold voltages, causes all of the outputs to go high. Therefore at time, $t_1 + t_{c1}$, all of the bits are high. The output of the MSB is one input to each of the D/A's on the two least significant bits. Also, the output of the second MSB is one input of the LSB's D/A. These voltages on the D/A inputs cause the threshold of the second MSB to go to six volts and the LSB threshold to go the seven volts. At time, $t_1 + t_c + t_{D/A1}$, the thresholds of the two least significant bits are at 6 and 7 volts respectively."

Since at this time the input voltage is less than the 2nd MSB's and LSB's comparator thresholds, both of the two least significant bits of the A/D go to logical 0. "Because the output of the second MSB is an input to the LSB's D/A, the threshold of the LSB again changes. At time, $t_1 + t_{c1} + t_{D/A2} + t_{c2} + t_{D/A3}$ the threshold of the LSB is at 5.0-volts. Since 5.0 volts is less than the 5.1-volt input, the output of the LSB goes high. The conversion is complete at time $t_1 + t_{c1} + t_{D/A2} + t_{c2} + t_{D/A3} + t_{c3}$. Thus, at this time the data outputs on the comparators is the digital representation of the input voltage."

Note that the MSB of the output is valid after only one comparator delay following the application of the input because the threshold of the MSB is a constant. Since one output to the NMSB is controlled by the MSB, the NMSB output cannot be assumed valid until one D/A settling time after the MSB becomes valid plus one comparator delay. (Therefore, two comparator delays and one D/A settling time are required before the NMSB can be considered valid.)

The above analysis can be applied to as many succeeding stages as desired to give the time necessary to insure the accuracy of a given

bit. In general, for an n-bit system, the maximum conversion time is given by [12],

$$T_{c(max)} = nt_c + (n-1)t_{D/A} \tag{5}$$

where n is the number of output bits.

The VTF converter determines the MSB first, followed by the NMSB, etc. If the A/D outputs were to be taken prior to the completion of the conversion, the errors would occur in the least significant bits only. Such errors would appear as if the system were bandwidth limited [12]. This does mean, however, that the system can give useful information before it has had time to complete a conversion. Note that the other A/D methods considered would yield totally unpredictable outputs if interrogated before the conversion time were complete.

In a VTF system, the conversion time is a function of the amount of change in the analog input since the last sampling occurred. For example, if the input voltage only changes by one least significant bit, the maximum conversion time would be only two comparator delays and a single D/A settling time.

CHAPTER IV

THE CCD A/D DESIGN

Various design schemes have been analysed, and the VTF A/D conversion scheme appears most amenable to CCD implementation. Figures 13 and 14 show an original design and the associated timing diagram for an 8-bit VTF A/D converter. This particular design is synchronous and can be totally implemented with CCD components. Note that Figure 13 makes use of analog as well as digital delay lines. Such a circuit would have been difficult to construct with previous technologies due to the presence of the analog delay lines; however, the advent of CCD technology has made circuits like Figure 13 practical.

The delay lines in Figure 13 are used to apply a standard sampling rate to a VTF system (e.g., the asynchronous VTF A/D discussed in Chapter III) and to assure that conversions are complete prior to their appearance at the output. In general for an n-bit converter, n-digital delay lines, and a single analog delay line are used to achieve synchronous operation. The time delay associated with each delay line element is equal to the clock period; the minimum clock period is determined by the restriction that it must be greater than the sum of a single comparator delay plus the time required for a D/A to settle. The purpose of the analog delay line is to allow the more significant bits to initiate a new conversion prior to the completion of the previous conversion that is still taking place in the least significant bit positions of the converter.

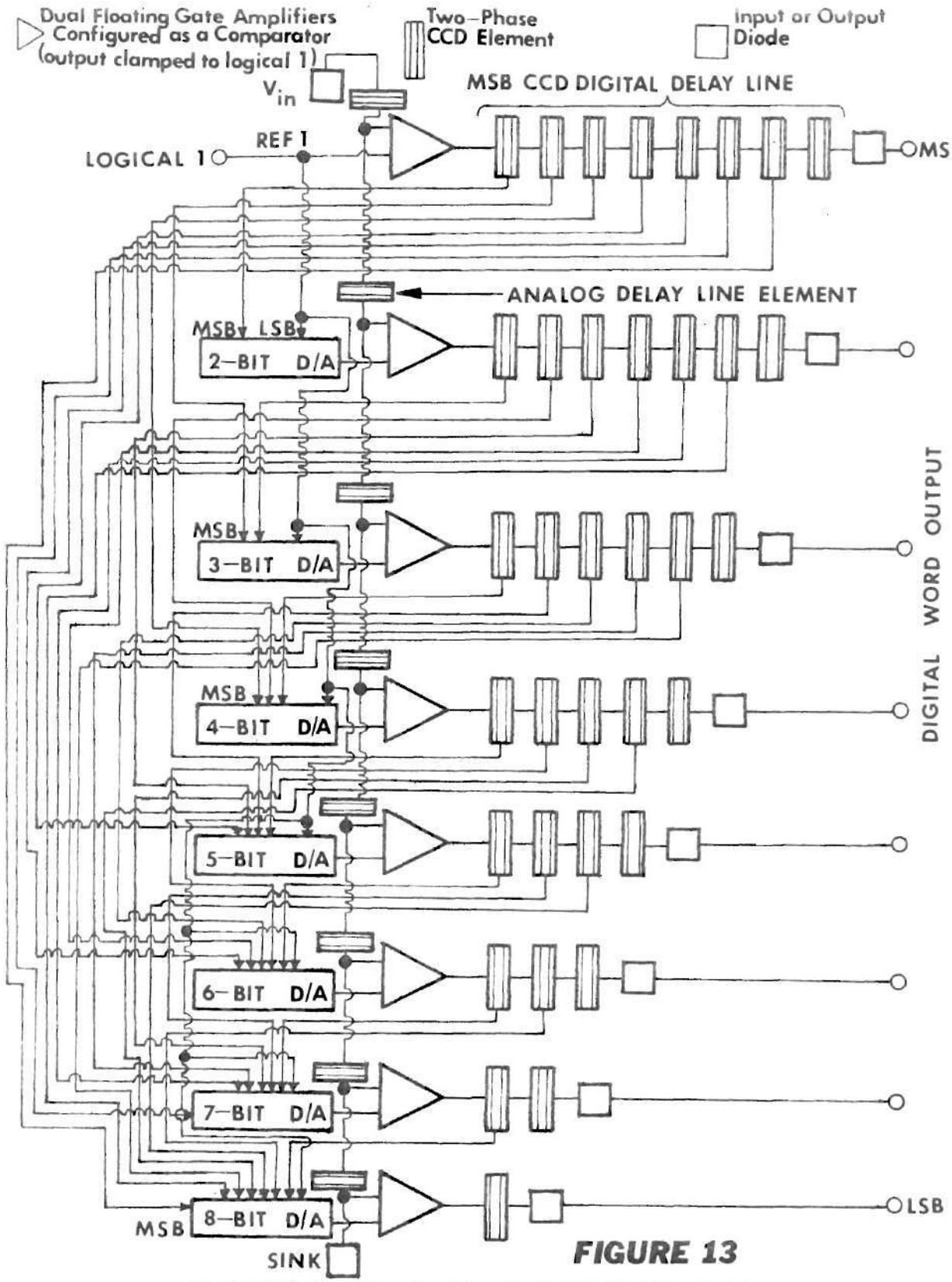


FIGURE 13

8-BIT CCD A/D CONVERTER

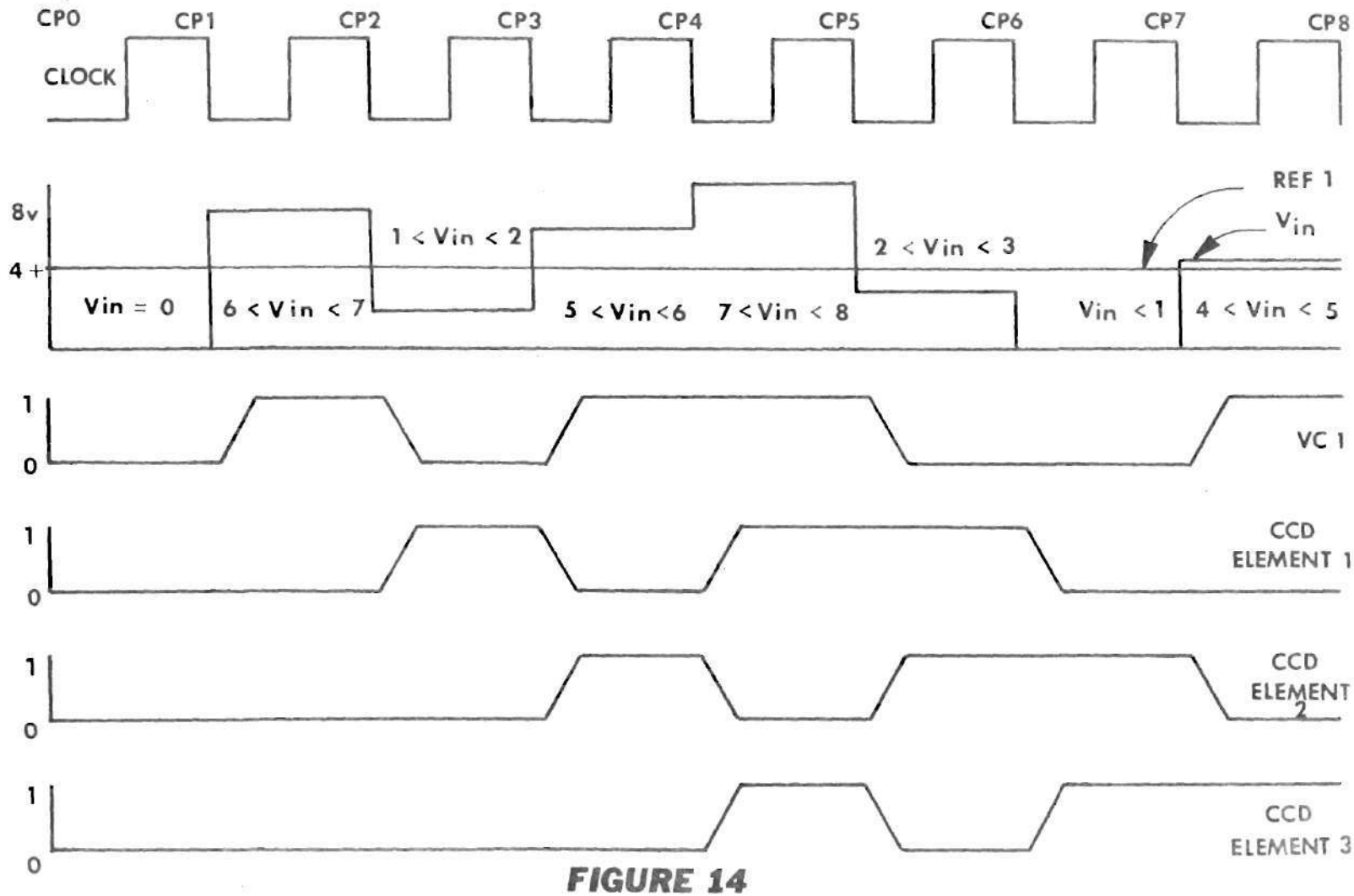


FIGURE 14

WAVEFORMS RELATED TO THE GENERATION OF THE MSB OF A VTF A/D

ELEMENTS IN DIGITAL DELAY LINE on MSB

Unlike the analog delay lines, the digital delay lines decrease in delay time ranging from n-clocktimes long for the MSB output, to a single-clocktime delay on the output of the LSB (see Figure 13).

The resulting output appears as a complete conversion every clock period after an initial delay of n-clock periods to allow the digital delay lines to fill up. Therefore, once the initial delay of n-clock times has occurred, complete n-bit A/D conversion words are clocked out at almost a real-time rate considering that the sum of one comparator delay and one D/A settling time amounts to only a few nanoseconds.

Synchronous VTF A/D conversion is ideally suited for CCD implementation since analog and digital delays are used concurrently. The design of Figure 13 and 14 for a CCD-VTF-A/D produces a system which exhibits high conversion speed, extremely low power requirements, simplicity of use, and low unit cost.

The power requirements for the CCD A/D are seen to be very small when the analysis of Kosonocky and Carnes [14] is applied to the circuit of Figure 13. If C_{ox} is defined as the capacitance of the channel oxide under a phase electrode, and C_s is defined as the effective capacitance of the corresponding depletion layer, then $C_{ox} + C_s$ represents the effective capacitance, C_E, of a phase electrode. According to Kosonocky and Carnes, C_{ox} is often more than an order of magnitude greater than C_s. Therefore the effective capacitance of the phase electrode reduces to the form of a simple parallel-plate capacitor. Assuming that the area of an electrode for one CCD element is 10^{-10} m^2 (A) and the channel oxide is 2000 Å thick (d), the capacitance of each phase electrode is found as

$$C_E = \varepsilon_{r_{SiO_2}} \varepsilon_o \frac{(A)}{(d)} \tag{6}$$

$$= \frac{(3.78) * (8.854 * 10^{-12}\ F/m) * (10^{-10}\ m^2)}{(2.0 * 10^{-7}\ m)}$$

$$= 1.67 * 10^{-14}\ \text{Farad}$$

This means that a charge signal of 10^{-13} coulombs will produce about a 6 volt surface potential change in a single CCD element. If the phase voltage is taken as 10 volts, the reactive energy per phase for one CCD element is

$$E = C_E V^2 \tag{7}$$

$$= (1.67 * 10^{-14}\ F)(10V)^2$$

$$= 1.67 * 10^{-12}\ \text{Joules}$$

For a clock rate of 10^7 Hz, the reactive power is

$$\text{Power (Joule/sec = watt)} = (E)(f_c) \tag{8}$$

$$= (1.67 * 10^{-12} J)(1 * L)^7\ \text{cycle/sec})$$

$$= 16.7\ \mu W/\text{element}$$

In relation to the circuit configuration of Figure 13, a two-phase clocking scheme (implying two CCD elements per delay-line bit) would result in the circuit power of

$$P_t = P_{CCD} + P_{comp} + P_{D/A} \tag{9}$$

where P_{CCD} = (16.7 μW/element * 44 elements * 2), and where it is estimated that the combined power consumption of the FGA comparators and the resistive D/A's (with their associated input buffers) is no greater than 500 μW. The total power consumption is therefore on the order of 2 mW. Present non-CCD integrated A/D converters require about 1 watt, or 500 times the expected power consumption of the CCD system.

Using today's technology, a monolithic circuit for Figure 13 could be fabricated. Production costs of IC devices are proportional to chip area. The electrode area of a CCD element was shown to be approximately 10^{-10} meters. The total chip area required to integrate the two-phase clocked CCD-VTF-A/D converter shown in Figure 13, (assuming diode input/output and resistive D/A's) is approximately $700 * 10^{-10}$ meters^2 (4600 mil^2). Since the area of a typical MSI transistor-transistor logic (TTL) chip is $1000 * 10^{-10}$ meters^2 (6400 mil^2), the cost of a monolithic CCD-VTF-A/D converter in production quantities, would be comparable to that of a standard MSI TTL device.

In addition to its low power consumption and reasonable chip size, the monolithic CCD-VTF-A/D converter could be placed in a single 14-pin dual-in-line (DIP) package. Eight pins could serve as digital outputs; one as the analog input; one pin as the reference voltage; two pins for the clock lines; one pin for supplying power to the floating gate amplifiers; and one pin serving as the ground terminal. A more universal configuration, however, would be to use a standard 24-pin DIP. This would permit two 8-bit CCD-VTF-A/D converters to be cascaded to produce a converter of up to 16-bits resolution. In the cascade arrangement, 14

of the pins would function as mentioned previously with eight of the remaining 10 pins used as D/A access ports and one pin each for an analog carry-out, and an analog carry-in. In order to cascade two of these chips, the circuit designer need only connect the eight output lines from the 'most significant chip', and connect the analog carry-out line of the MS-chip to the analog carry-in line of the LS-chip. Cascading of two such identical 8-bit chips could effectively produce a converter of up to 16-bit capacity.

Further simplifying the use of the CCD-VTF-A/D converter is its unidirectional shifting property that allows the use of a two-phase clock rather than the harder to generate three-phase clocking that becomes necessary in bidirectional CCD devices. (A more detailed discussion of the utility of various clocking schemes can be found in Appendix II).

The performance of the CCD-VTF-A/D converter was evaluated by constructing a computer simulation capable of modeling the circuit configuration of Figure 13. The next chapter describes the simulation program.

CHAPTER V

THE SIMULATION PROGRAM

The CCD-VTF-A/D converter of Figure 13 will be modeled using transfer functions for the digital and the analog shift registers, the D/A converters, the comparators, and the input and output diodes. The effects of transfer efficiency, clock frequency, and temperature will be included in the transfer function derivations.

Consider first the derivation of the transfer function for an n-bit CCD delay line (i.e. an n-bit shift register). According to TRW [19] the signal charge of a CCD delay line may be calculated from the following discrete recursion formula

$$q\ (x,\ t) = \varepsilon q_s(x,\ t-1) + (1-\varepsilon)q_s(x-1,\ t-1) \tag{10}$$

where ε is the transfer inefficiency (i.e. that part of the signal charge which is left behind), t is time, and x is distance along the delay line. Equation (10) represents a discrete set of signal values in the time domain, and therefore may be transformed into the Z-domain.

$$Q_s(x,\ Z) = Z^{-1}\ [\varepsilon Q_s(x,\ Z) + (1-\varepsilon)Q_s(x-1,\ Z)] \tag{11}$$

where $Z = e^{ST_c}$, $S = \sigma + j\omega$ the complex frequency, and $T_c = 1/f_c$ the clock period. Equation (11) may be rearranged into the form

$$\frac{Q_s(x,\ Z)}{Q_s(x-1,\ Z)} = \frac{(1-\varepsilon)Z^{-1}}{1-\varepsilon Z^{-1}} \tag{12}$$

From the definition of capacitance, the input charge to a CCD delay line may be written as

$$Q_s(0,\ Z) = C_{in}V_{in}(Z) \tag{13}$$

where C_{in} is the storage capacitance associated with the input charge injection circuit (e.g. P-N junction). In general, the output of a CCD delay line is isolated with a buffering amplifier. This buffer amplifier has a gain of $g_m R_L$ where g_m is the amplifier's transconductance and R_L is the load resistance. If the output capacitance C_{out} of the buffer is known, the transfer function of the output buffer can be written as

$$V_{out}(Z) = \frac{g_m R_L Q_s(n,\ Z)}{C_{out}} \tag{14}$$

Combining equations (12), (13), and (14), the overall transfer function for an n-bit CCD delay line becomes

$$H(Z) = \frac{V_{out}(Z)}{V_{in}(Z)} = \frac{g_m R_L C_{in}}{C_{out}} \left[(1-\varepsilon)/(1-\varepsilon Z^{-1})\right]^n Z^{-n} \tag{15}$$

In general, $\varepsilon << 1$, and equation (12) reduces to

$$H(Z) = H_o Z^{-n} e^{-n\varepsilon(1-Z^{-1})} \tag{16}$$

where $H_o = g_m R_L C_{in}/C_{out}$. Note that H_o is a constant and can be normalized to unity by assuming the gain of the buffer amplifier is unity and the input capacitance is equal to the output capacitance. The frequency behavior of the sampled data CCD delay line can be obtained from equation (16) with the substitution

$$Z = e^{j\omega T_c} = e^{j2\pi f_s/f_c} \tag{17}$$

where f_s is the signal frequency and f_c is the clock frequency. The resulting magnitude and phase functions are

$$|H(f_s)| = e^{-n\varepsilon(1-\mathrm{Cos}(2\pi f_s/f_c))} \tag{18}$$

$$\angle H(f_s) = \frac{-2n\pi f_s}{f_c} - n\varepsilon \mathrm{Sin}(2\pi f_s/f_c) \tag{19}$$

The Sampling Theorem imposes the constraint that $f_s \leq 0.5 f_c$. Equations (18) and (19) can be applied to both the analog and digital shift registers since the only difference lies in the way in which the output data is interpreted.

The leakage current in a CCD limits the maximum time delay possible by degrading the dynamic range. Leakage currents are generated via several mechanisms; however, thermal sources are usually the dominant generators. The temperature dependence of the leakage current is

determined by the expression [19]

$$I_L = I_{LO} e^{-\frac{E_G}{2k}[1/T - 1/T_o]} \tag{20}$$

where I_{LO} is the leakage current at a temperature of $T_o = 298°$ K (typically on the order of 1 nA), E_G is the potential of the silicon band gap (1.11 V), and k is Boltzmann's constant ($k = 8.5 * 10^{-5}$ J/V). It is assumed that the charge added to each potential well due to thermally generated minority carriers is constant for each well regardless of its orientation.

In the simulation program the transfer function response and the effects of thermally generated leakage currents are modeled by considering how much of the total charge is transferred from one element into the next. The residual charge left behind in an element must be added to the incoming charge. In addition, the charge generated by thermal effects must be considered as a part of the total charge content of each CCD element. A FORTRAN implementation of the transfer function and thermal response is of the form

$$V_n = V_{n-1}|H(f_s)| + (V_n - V_n|H(f_s)|) + V_{therm} \tag{21}$$

where V_n is the voltage proportional to the charge in CCD element n, and V_{therm} is the potential increase due to thermal leakage currents. Two-phase clocking will be simulated with the result that Equation (21) is based on n = 2 element groupings.

The comparators having already had their output characteristics accounted for as the input to the digital delay lines, need only be represented as a FORTRAN IF statement. This IF statement compares the outputs of the various D/A converters with the corresponding analog CCD delay-line elements. The outcome of this decision process results in either a logic 1 or a logic 0 being injected into the digital delay line upon the occurrence of the next clock pulse.

The D/A converters are implemented by weighting their inputs according to bit position. The D/A's are assumed to be resistive ladder networks with input buffering which makes them free from the effects of thermal minority carrier generation and transfer inefficiency that would have to be considered in a totally CCD D/A implementation.

The data inputs and outputs are assumed to be of the P-N junction type. All data flow into or out of the A/D converter is directly into or derived directly from the CCD delay lines; therefore all data ports have their effects accounted for by the CCD delay-line transfer function.

In the next section, the results of the CCD-VTF-A/D simulation are given for various temperatures and clock frequencies. These results point out important conclusions concerning the overall operation of the converter.

CHAPTER VI

SIMULATION RESULTS

A sample run of the simulation program is presented in Appendix IV. The parameters for this particular run were chosen to be close to those that might be encountered under actual operating conditions:

Clock Frequency: 100 MHz
Logic 1 Reference Level: 0.25 V
Substrate Temperature: 25° C
Transfer Efficiency $(1-\varepsilon)$: 0.9999

Worse case conditions for the f_s/f_c ratio in the CCD transfer function occur when the converter is operated at exactly the Nyquist rate; therefore f_s/f_c was set equal to 0.5 which causes maximum amplitude and phase deviation.

Appendix IV shows that when the first clock pulse (CP(1)) is applied, there is an initial amount of charge present in both the digital and analog delay lines. This is due to the thermally generated minority carriers located within a diffusion length of each of the CCD elements. As stated earlier, it is assumed that the thermal generation of charge is identical for all CCD elements during a given interval of time. The simulation results corresponding to the CCD delay lines represent the voltages that would accumulate due to the influx of thermally generated charge during one clock period $(1/f_c)$. When the second pulse occurs (CP(2)), the accumulated charge is shifted toward the output of the delay line with the result that

the charge in the first CCD element moves into the second element, charge in the second to the third, and so on. The charge in the final element is shifted to a load element as an output signal. After this shift has been completed, the effects of the thermally generated charge again must be considered as charge is added equally to each potential well. Note that this thermal charge adds to that charge left behind from the previous transfer. This process continues for each clock period until a uniform charge gradient is formed. This gradient is of constant slope, monotonically increasing from the first element in the delay line to the final element. The constant gradient occurs because as more thermally generated charge enters the delay line, it is constantly swept toward the output. CP(22) shows the steady-state trend of the leakage-charge gradient. At steady state, the value of the accumulated leakage charge in any element is twice the charge that is present in the previous element, or

$$Q(n) = 2Q(n-1) \tag{22}$$

The effect of the thermally generated charge gradient worsens as the length of the delay line is increased. For the CCD-VTF-A/D, the thermal charge gradient causes an error in the least significant bit of the converter since the LSB is derived from the final stages of one of the two longest delay lines in the converter (the 8-bit analog-delay line). This conclusion was apparent in all of the simulator data runs in which errors occurred.

The MSB is the most suspect for causing inaccuracies since it is derived from the longest digital delay line. Indeed this would be the case were it not for the inherent noise immunity of digital devices. The delay of the MSB digital CCD line is equal to the delay of the analog line, and therefore the thermal charge gradients are equivalent. However the digital CCD delay line output is compared with a threshold voltage while the analog CCD delay line output must be measured exactly. This difference makes the CCD components whose inputs are derived from the analog delay line much more susceptable to the effects of thermal leakage currents than those associated with the digital delay line.

Figure 15 shows a family of curves representing the probability of bit error versus frequency for several different temperatures. The probability of bit error is the rate of k/m such that k bits will be in error during a run involving a total of m bits. For a low clocking frequency (long period), each CCD element accumulates more thermally generated charge per data packet than it does when the clocking frequency is high. With a high clock frequency, the data packets are being shifted in and out of the delay lines too fast to allow much thermally generated charge to be picked up. From Figure 15 it can be seen that the slope of the curves is a maximum in the vicinity of 0.5 bit error probability. This behavior can be attributed to the digital nature in which the output values are interpreted. The voltages corresponding to the amount of charge in each of the digital delay-line outputs (being interpreted as digital information by any devices connected to the A/D outputs), are compared to a threshold voltage in order to determine a logic 0 or a logic 1. The thermally generated minority carriers that constantly collect in the CCD

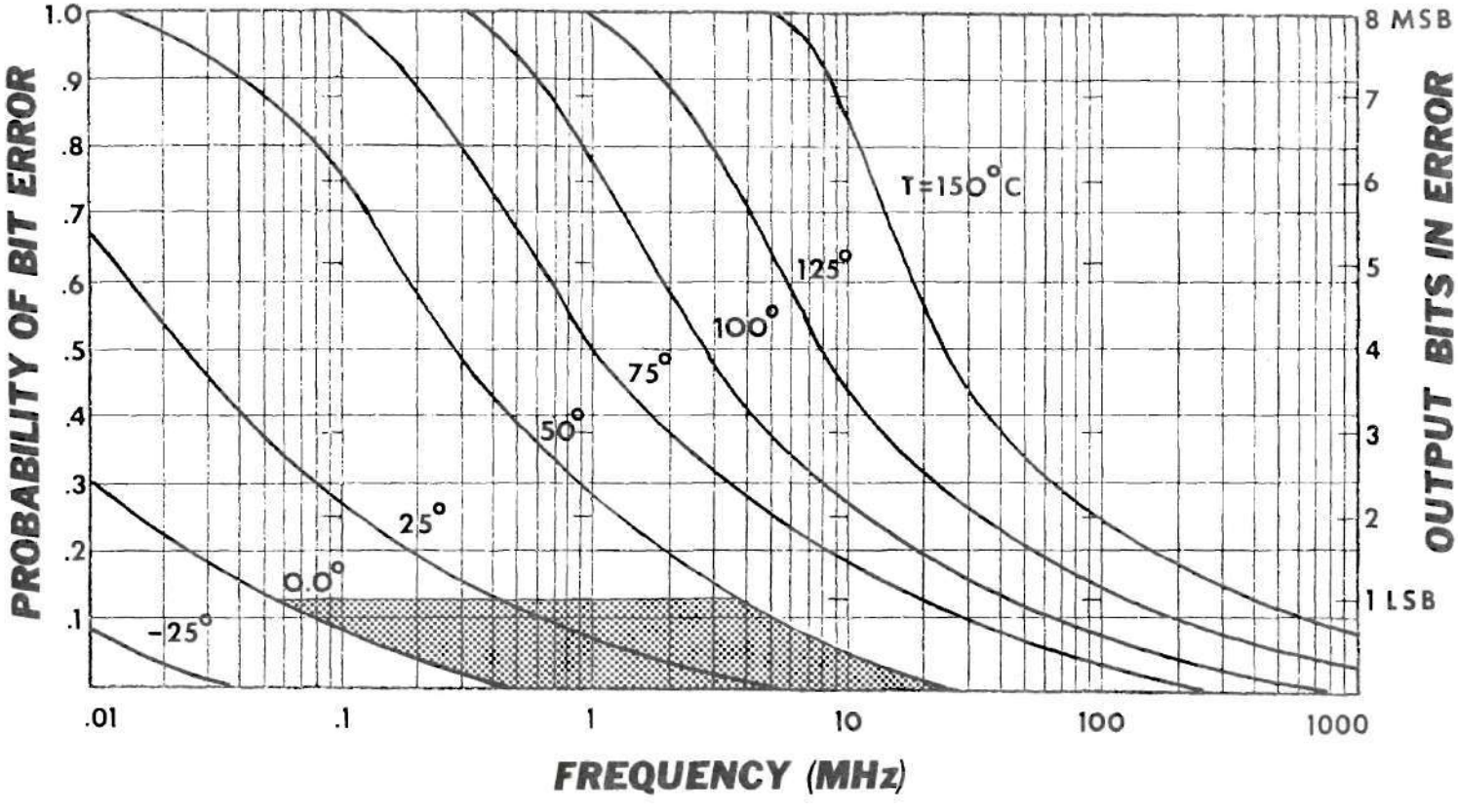


FIGURE 15

PROBABILITY OF BIT ERROR vs FREQUENCY

elements will have no effect on this comparison until sufficient charge causes what would normally be interpreted as a logic 0 to surpass the threshold level. When this happens, a bit error has occured. Since each digital delay line in the CCD-VTF-A/D differs by only a single pair of elements (two-phase clocking implies element groupings of two), only a minor variation in clock frequency or temperatures will cause the next least significant bit to be in error. As a result, most bit error will occur within a localized region for any given clock frequency and temperature.

The slope of the bit error probability can be reduced somewhat by tailoring the output threshold comparison voltages of subsequent digital devices to the corresponding CCD-VTF-A/D outputs. This can be done because of the predictable nature of the thermally generated minority carrier gradient at each output of the A/D. The output statements of the simulation program have been tailored to take advantage of this predictability.

Another mechanism that contributes to the behavior of the CCD-VTF-A/D converter is the propagation delay through the asynchronous parts of the system such as t_c and $t_{D/A}$. In the simulation program these propagation delays were assumed to be zero. In an actual device, these delays, along with the effects of capacitance between data lines, would tend to limit the high frequency conversion rate. Recalling Equation (5), the maximum conversion time for a VTF A/D converter was shown to be

$$T_{c(max)} = nt_c + (n - 1)t_{D/A} \tag{23}$$

Present technology is capable of producing 8-bit D/A converters with settling times ($T_{D/A}$) on the order of 25 nsec to $\pm$ 0.1 % of full scale. Comparator response times (t_c) depend principally upon the capacitive loads that they drive. In the case of the CCD-VTF-A/D, the comparators drive the capacitance of the first CCD elements in the respective digital delay lines. This capacitance was shown to be on the order of 10^{-14} Farad. For a silicon substrate resistivity of ρ = 10 Ωcm, the RC time constant can be calculated by noting that

$$R = \rho \frac{\ell}{A} \tag{24}$$

where ℓ is the interelectrode spacing and A is the cross-sectional rate of current flow into the inversion region beneath a CCD element. According to Amelio [2], "a preferred structure should possess an electrode-length-to-(interelectrode) gap-length ratio of about unity." It was stated earlier that a typical electrode area is 10^{-10} meter^2. Assuming the electrodes are square gives the electrode lengths as 10^{-5} meter. Kosonocky and Carnes [14] show that this time constant would be on the order of 10^{-9} seconds for a buried* N-channel device. Since this charge transfer is expected to follow an exponential time relationship, the potential well will be filled to about 99 percent of its maximum voltage in about five time constants, or 5 * 10^{-9} seconds. Using this value for t_c, it can be shown by Equation (23) that for an 8-bit CCD-VTF-A/D converter, the maximum theoretical conversion time is about 215 nsec. which corresponds

*See Appendix I

to a conversion rate of somewhat more than 4.6 MHz. Therefore, the CCD-VTF-A/D converter (using resistive D/A's) has a conversion frequency between that of the parallel converter and that of successive-approximation. This result is expected since the limiting factors are presently the propagation delays of the comparators and the D/A's (i.e. the non-CCD components). Note that this result is the maximum theoretical conversion time, and is therefore a worse case indicator. As stated previously, the most significant bits of an asynchronous VTF converter are the first to become valid. In the case of the synchronous CCD-VTF-A/D, the conversion frequency could be increased if bit errors in the least significant bits can be tolerated. For example, if high confidence were placed in only the first four bits of the converter output, the CCD-VTF-A/D could be reliably clocked at more than 10.5 MHz.

Thus far, it has been assumed that the input data is permitted to change drastically from sample to sample; this is another worse case condition. Recognizing that the maximum conversion time is also dependent on the rate of change of the input signal, the conversion rate of the CCD-VTF-A/D could be raised much higher than the estimated 4.6 MHz clock rate if it were known that all of the analog input data lies within a small portion of the system's dynamic range.

CHAPTER VII

CONCLUSIONS

The results of this work have shown that an 8-bit CCD A/D could be designed which incorporates the desirable properties of several conversion techniques. A simulation program permitted the evaluation of the CCD-A/D design as a function of temperature, transfer efficiency, and clock rate. The simulation results showed that the effects of temperature and clock rate are closely related.

Transfer efficiency was found to be of less importance due to the relatively short delay lines employed in the converter. Data was obtained from the simulation program for a wide range of temperature-clock rate combinations. This data reveals regions of operation subject to given sets of constraints. For example, if the commercial temperature range of 0 - 50° C is considered, the CCD-VTF-A/D is constrained to operate in the shaded region of Figure 15 to obtain full 8-bit accuracy.

Analysis of the time constants associated with the various components showed that the maximum theoretical conversion time was approximately 215 nsec. The CCD-VTF-A/D converter is faster than many successive-approximation schemes, but somewhat slower than a parallel converter. A conversion time of 215 nsec. corresponds to a conversion rate of more than 4.6 MHz. This conversion rate represents a worse case condition, and the converter is capable of higher conversion rates if the analog input signal is relatively constant, or if some of the least significant bits can be neglected. The factors preventing conversion rates of 100 MHz

or more, can be attributed to the non-CCD components; in particular the D/A's. In order to achieve higher conversion rates, a faster D/A technique must be devised, and the geometry of the CCD elements must be modified such that the comparators drive less of a capacitive load.

Standard packaging techniques can be employed to encase the CCD-VTF-A/D converters and would provide no major inconveniences to the designer who wished to use such devices.

Economically, a monolithic 8-bit CCD-VTF-A/D was shown to be comparable in chip area to standard TTL MSI, and it was therefore estimated that a CCD-VTF-A/D such as this would also be of comparable cost in production quantities.

As well as demonstrating utility, versatility, and potential economy, it was shown that the power requirements for a monolithic CCD-VTF-A/D converter would be approximately 2 mW, or a 500 percent reduction over the power required for present converters. This, coupled with its small size and good speed/cost ratio, makes the CCD-VTF-A/D converter a viable state-of-the-art alternative to present A/D converters.

Recomendations For Further Work

This research indicates the need for further work in several areas. Since the maximum conversion rate of a CCD-VTF-A/D is, at present, primarily limited by the delays associated with the comparators and D/A's, additional investigation is needed to look into the exact mechanism involved in these propagation delays. A totally CCD-D/A implementation might prove beneficial.

Additional study is needed to refine the CCD-VTF-A/D simulation routine to account for propagation delays through the asynchronous components of the converter. The effects of various clocking waveforms might also be modeled. If it were found that a totally CCD-A/D implementation was advantageous, an analysis similar to that of the CCD delay lines could be performed on the D/A's, and the simulation routine modified accordingly. Certain second order effects such as lateral charge leakage from a CCD element might be included in the simulation program as well.

In summary, this thesis has presented an original design using charge-coupled devices to achieve analog-to-digital conversion. Simulation results have demonstrated that the CCD-VTF-A/D converter is functionally operational. These results provide additional insight into the system's operation and open the door for extended research investigation to be conducted with CCD converters.

APPENDIX I

GLOSSARY OF CCD AND ANALOG-TO-DIGITAL CONVERSION TERMINOLOGY

1. ACCURACY [12]

Accuracy must include all of the sources of errors (quantization, non-linearity, noise, and short term drift). Relative accuracy is often defined as the deviation from a straight line passing through zero and the nominal full scale value (very similar to linearity). A typical accuracy specification might be 0.05% $\pm \frac{1}{2}$ LSB at + 25°C.

Long term stability, not included in the accuracy specification, defines the additional error introduced because of component aging. It is measured over a period of time (generally one to three months) at a fixed ambient temperature. A typical long term stability specification might be ± 0.005%/90 days at + 25°C.

2. AMPLIFIER SETTLING TIME [12]

Amplifier settling time is the interval required for the output of an amplifier to become stable after the application of a step-function input. An output is considered stable when it has recovered from its transient response to such a degree that its output approaches its steady state value within plus or minus one least significant bit (LSB). Total settling time may include sample and hold time, multiplexing time, converter settling time, plus the actual conversion time. Conversion time specifications must be read carefully as some may include all, and others only part of the above mentioned.

3. APERTURE [12]

Aperture is the amount of uncertainty about the exact time when the encoder input was at the value represented by a given output code. In general, the aperture is equal to the conversion time. However, with the use of a sample-and-hold circuit as an input network, the aperture can be reduced, since more information is known about when the input sample was obtained relative to the timing of the output result.

4. BIT-PERIOD [12]

The bit-period is determined by dividing the conversion time by the number of bits employed in the conversion. A bit-period of

less than two microseconds per bit is generally considered to be high speed operation.

5. BURRIED CHANNEL [7]

Because charge trapping can occur at the surface of the $Si-SiO_2$ interface, a thin doped layer can be introduced in the silicon just below the oxide (typically by ion implantation) to prevent trapping of charges.

6. CHANNEL DIFFUSION STOPS [7]

A narrow, doped region beside each sensing channel that prevents excess charges generated within a particular site from spreading sideways.

7. CHARGE COUPLING [9]

A method of moving finite charge-packets of electrons (in P-type silicon; holes in N-type silicon) from one position in the semiconductor to an adjacent position by the use of sequential gate induced depletion regions (potential wells) and electric fields. The packets of charge are minority carriers and no junctions are required, thus providing low noise level operation.

8. CHARGE TRANSFER EFFICIENTY [9]

The degree to which the entire charge packet of electrons is moved from one potential well to the next without loss.

9. CONVERSION ERROR [12]

The discrepancy between the actual output of an analog-to-digital converter and the exact digital representation of the quantity being measured at the instant of measurement is conversion error. It is generally one-half of the value represented by the least-significant-bit.

10. CONVERSION RATE [12]

Conversion rate is a measure of the frequency at which conversions are made. It must take into account not only the conversion time, but recovery time as well, and will usually be less than the reciprocal of conversion time.

11. CONVERSION TIME [12]

In general, conversion time is that interval required for the converter to generate a digital representation of the input voltage. For programmed converters, conversion time is the elapsed time

between a command to perform a conversion, and the appearance at the converter output of the complete digital representation of the input voltage. For continuous tracking encoders, conversion time is the interval between a significant change occurring at the input, and that point at which the output settles to its new value. If an amplifier is used to drive the converter, the settling time of the amplifier is also to be included in the conversion time.

12. DECODER [12]

A decoder is a digital-to-analog (D/A) converter. (More commonly a monolithic D/A converter.)

13. DYNAMIC RANGE

The ratio of the saturation signal level and the minimum signal level detectable above the background electronic noise level.

14. ENCODER [12]

An encoder is an analog-to-digital (A/D) converter. It is also referred to as a digitizer, or as a quantizer.

15. FAT ZERO [7]

In surface channel CCD's, charge tends to be captured by surface effects, thus resulting in a loss of signal. By continuously introducing a charge into all CCD channels through a diffusion at the beginning of the channel, the areas that trap charges are filled by the induced charges rather than the signal charges, thus increasing transfer efficiency.

16. INPUT IMPEDANCE [12]

The input impedance of the converter system is the amount of load that the ADC represents to its source; the quantity being measured. A typical comparator with a 50 MΩ input resistance will load a source resistance of 1 kΩ sufficiently to introduce an error of 0.002%.

17. LINEARITY [12]

Linearity is a measure of the deviation from a straight line of a plot of the input-output ratio of an analog-to-digital converter over its operating range and is usually expressed in a percent of full scale.

18. MIS;METAL-INSULATOR-SILICON [7]

A technology wherein a silicon dioxide layer is formed on a single crystal silicon substrate and a polysilicon conductive is

formed on the oxide. This layer is etched to form the electrode pattern and then doped with phosphorous to create the desired conductivity.

19. MONOTONICITY [12]

Monotonicity relates to an increasing output for every increasing value of input voltage. Another way of saying this is that the derivative of the output with respect to the input is always positive. A converter must be capable of producing every coded value within the input range defined. The accuracy of the various resistors in the digital-to-analog converter ladder network and the offset voltage in the switching electronics must be minimized, so that the sum of the errors for any given number of successive lesser significant bits is less than the error produced by the next most significant bit; otherwise, it would be possible to force non-uniform spacing of the quantum levels and miss some of the output codes altogether. Absolute requirements for monotonicity are that all codes are obtainable and that the quantization level of each code be within one-half of one least-significant-bit of the ideal, linear-related quantization level.

20. POLYSILICON [7]

A multicrystalline form of silicon used in silicon gate MOS technology that is electrically conductive and optically transparent.

21. POTENTIAL WELLS [7]

A voltage placed on MIS capacitor electrodes causes a voltage gradient zone to be formed under the electrode so as to collect minority carriers.

22. PRECISION [12]

Precision relates to the repeatability of successive measurements. Precision is limited in practice by noise and a small but finite quantization error that always exists in some "dead band" at each successive numerical value. When the unknown analog voltage lies within any of the dead bands around each of the possible values, the repeatability can never be greater than plus or minus one least-significant-bit. One measure of the quality of the high speed analog-to-digital converter is the ratio of the dead band to the full quantization level for each value across the entire range.

23. QUANTUM LEVEL [12]

In an n-bit encoder there are exactly 2^n different states. If the analog reference voltage is divided into 2^n parts then one part represents a quantum of voltage. The reference voltage is

quantized into 2^n quantum levels where each quantum level is represented by one of the 2^n binary states in an n-bit quantizer.

The error of quantization is a function of the number of bits in the converter. An A/D converter is normally adjusted for the center of each of the binary weighted steps; hence, the error of quantization is at most one-half of a significant bit ($\frac{1}{2}$ LSB).

24. RESOLUTION [12]

Resolution is the ability of the converter to distinguish between adjacent values of the quantity being measured. Normally the resolution would be considered to be limited only by the number of bits carried. In practice, however, the ultimate resolution of a given design is limited by the noise in the various analog and switching circuits, and by the linearity and monotonicity of the converter. Specifications for the resolution of a converter should be compatible with the number of bits and vice-versa, otherwise the specification would imply that the readings convey a higher degree of resolution than could actually exist.

25. SAMPLE AND HOLD [13]

Circuitry for sampling the value of an analog voltage for a given period of time, and, after the sampling is complete, storing the analog voltage for the required holding time. It can be used to reduce the aperature time of A/D converters.

26. STABILITY [12]

The factor of stability simply relates to the ability of the converter to maintain the characteristics (relative accuracy, resolution, precision, etc.) over a defined operating interval. Lack of stability occurs primarily for two reasons: drift in the voltage reference and the resistors, and drift in the conversion switching networks.

27. STEPPED OXIDE [7]

A technique of forming the SiO_2 layer of each electrode in two thicknesses so that a two-level potential well can be formed with one voltage.

28. SURFACE CHANNEL [7]

The potential well of a CCD is formed at the Si-SiO_2 interface and the transfer occurs near the interface.

29. THROUGHPUT RATE

Same as conversion rate.

APPENDIX II

CLOCKING SCHEMES [19]

"The clocking scheme design is concerned with two items: the clock voltage wave-form and the number of clock phases. It is generally true that two-phase clocks imply more power dissipation than clocks of three or more phases, simply because two-phase clocks depend on a built-in asymmetry to ensure charge flow directionality rather than depending on phasing alone. However, the added power advantage of going to multi-phases is slight and is generally more than offset by the added complexity of generating and applying several clock signals. TRW and others have experimentally demonstrated that two-phase clocks are realizable by a simple arrangement of a dc voltage for one phase and an ac voltage for the second phase, with proper amplitude adjustments to ensure charge transfer. This scheme completely avoids any phasing problems and requires generating only one clock waveform.

The actual shape of the clocking waveform is important. The power dissipated in the clock driver is a function of the voltage waveform. Table 2 indicates the relative clock driver dissipation for three common configurations: squarewave clock drivers, untuned sinewave clock drivers, and tuned sinewave clock drivers. Tuned clock drivers have the best potential for low power dissipation, if high values of circuit Q can be obtained; they are, in general, more complex circuits and they require inductors making a completely integrated driver difficult if not impossible. Squarewave and untuned sinewave drivers can be constructed in integrated form; however, precise sinewave waveform amplitude control is more difficult than squarewave amplitude control. The relative power dissipation difference between untuned sinewave and squarewave drivers is normally not significant."

Table 2 [19]

Relative Power Dissipation for Several

Clock Driver Configurations

Configuration	Relative Value of Dissipated Power
Squarewave driver	High
Sinewave (untuned)	Medium
Sinewave (tuned)	Low

APPENDIX III

SIMULATION PROGRAM

```
C          ************* EXECUTIVE TIMING *************
      DIMENSION DCCDE(16,16),ACCDE(16),ANIFCN(512),DIODE(16),
     2SCAN(512),COMP(16),DTOA(16,16),UM(512),FRNUM(512),
     3DSA(16),OUTPUT(16)
      INTEGER CSIMNO,TEST,CLEAR1,CLEAR2,CP
1     FORMAT(A1,A1,A1,A1,I3,F7.3,F7.3,F10.4,F7.2)
      READ(5,1)DECPNT,BLANK,R1,RO,CSIMNO,REFLEV,TEMP,CKFREQ,FSUBS
      PCLOCK=CKFREQ
      CKFREQ=CKFREQ*1000000.
      FSUBS=FSUBS*1000000.
5000  FORMAT(////)
5001  FORMAT(9X,'**************************************************')
5002  FORMAT(9X,'*                                                *')
5003  FORMAT(9X,'*          CCD-VTF-A/D SIMULATION PROGRAM        *')
5004  FORMAT(9X,'*                                                *')
5005  FORMAT(9X,'**************************************************')
5006  FORMAT(///)
5007  FORMAT(' THE FOLLOWING PARAMETERS HAVE BEEN SELECTED:')
5008  FORMAT(/)
5009  FORMAT(' NO. OF CLOCK TIMES TO BE DISPLAYED:',I3)
5010  FORMAT(' CLOCK FREQUENCY:',F10.4,'  MHZ')
5011  FORMAT(' LOGIC 1 REFERENCE LEVEL:',F7.4,'  VOLTS')
5012  FORMAT(' SUBSTRATE TEMPERATURE:',F7.3,'  DEG. CELCIUS')
5013  FORMAT(//)
5014  FORMAT(' THE FOLLOWING',I3,'  PAIRS OF NUMBERS REPRESENT THE')
5015  FORMAT(' SAMPLED ANALOG INPUTS TO THE CONVERTER AND THEIR')
5016  FORMAT(' CORRESPONDING IDEAL BINARY VALUES:')
5017  FORMAT(/)
      WRITE(6,5000)
      WRITE(6,5001)
      WRITE(6,5002)
      WRITE(6,5003)
      WRITE(6,5004)
      WRITE(6,5005)
      WRITE(6,5006)
      WRITE(6,5007)
      WRITE(6,5008)
      WRITE(6,5009)CSIMNO
      WRITE(6,5010)PCLOCK
      WRITE(6,5011)REFLEV
      WRITE(6,5012)TEMP
      WRITE(6,5013)
      WRITE(6,5014)CSIMNO
      WRITE(6,5015)
      WRITE(6,5016)
      WRITE(6,5017)
```

```
2       FØRMAT(10F7.3)
        READ(5,2)(ANIFCN(TEST),TEST=1,CSIMNØ)
        DØ 3 TEST=1,CSIMNØ
        DØ 333 N=1,510
        UM(N)=BLANK
333     FRNUM(N)=BLANK
1000    INTEGR=INT(ANIFCN(TEST))
1001    FRAC=ANIFCN(TEST)-INTEGR
1002    N=1
1003    IDIV=INTEGR/2
1004    ICHECK=2*IDIV
1005    IF(INTEGR-ICHECK)7777,1006,1010
1006    UM(N)=RØ
1007    INTEGR=IDIV
1008    N=N+1
1009    GØTØ 1015
1010    UM(N)=R1
1011    INTEGR=IDIV
1012    N=N+1
1015    IF(IDIV.NE.Ø) GØTØ 1003
1016    MAXN1=N-1
1017    N=1
1018    FRACAN=2.*FRAC
1020    IF(1.-FRACAN)1030,1030,1025
1025    FRNUM(N)=RØ
1026    FRAC=FRACAN
1027    N=N+1
1028    GØTØ 1040
1030    FRNUM(N)=R1
1032    FRAC=(FRACAN-1.)
1034    N=N+1
        IF(N.EQ.12)GØTØ 1050
1040    IF(FRACAN-Ø.)1050,1050,1018
1050    MAXN2=N-1
        DØ 341 N=1,250
        SCAN(N)=FRNUM(251-N)
341     SCAN(251+N)=UM(N)
        SCAN(251)=DECPNT
331     FØRMAT( '     ',F7.6,'     ..............',41A1)
        WRITE(6,331)ANIFCN(TEST),(SCAN(271-N),N=1,41)
3       CØNTINUE
4       DØ 5 CLEAR1=1,16
        DØ 5 CLEAR2=1,16
        DCCDE(CLEAR1,CLEAR2)=Ø.
        ACCDE(CLEAR1)=Ø.
        DTØA(CLEAR1,CLEAR2)=Ø.
        ØUTPUT(CLEAR1)=BLANK
        CØMP(CLEAR1)=Ø.
5       DIØDE(CLEAR1)=Ø.
8000    FØRMAT(///)
8001    WRITE(6,8000)
        DØ 4444 CP=1,CSIMNØ
C
C
```

```
C       ************ BEGIN D/A SIMULATOR ************
C
        DTOA(1,8)=REFLEV/2.0
C
        DTOA(2,8)=DCCDE(1,1)/2.0
        DTOA(2,7)=REFLEV/4.0
C
        DTOA(3,8)=DCCDE(1,2)/2.0
        DTOA(3,7)=DCCDE(2,1)/4.0
        DTOA(3,6)=REFLEV/8.0
C
        DTOA(4,8)=DCCDE(1,3)/2.0
        DTOA(4,7)=DCCDE(2,2)/4.0
        DTOA(4,6)=DCCDE(3,1)/8.0
        DTOA(4,5)=REFLEV/16.0
C
        DO 2000 M=1,4
2000    DTOA(5,9-M)=DCCDE(M,5-M)/2.0**M
        DTOA(5,4)=REFLEV/32.0
C
        DO 2001 M=1,5
2001    DTOA(6,9-M)=DCCDE(M,6-M)/2.0**M
        DTOA(6,3)=REFLEV/64.0
C
        DO 2002 M=1,6
2002    DTOA(7,9-M)=DCCDE(M,7-M)/2.0**M
        DTOA(7,2)=REFLEV/128.0
C
        DO 2003 M=1,7
2003    DTOA(8,9-M)=DCCDE(M,8-M)/2.0**M
        DTOA(8,1)=REFLEV/256.0
C
        DO 1060 I=1,8
1060    DSA(I)=DTOA(I,1)+DTOA(I,2)+DTOA(I,3)+DTOA(I,4)+DTOA(I,5)+DTOA(I,6)
       4+DTOA(I,7)+DTOA(I,8)
C
C
C       ************ BEGIN COMPARATOR SIMULATION ************
C
        IF (ACCDE(1)  -DSA(1)) 1070,1075,1075
1070    COMP(1)=0.0
        GOTO 1076
1075    COMP(1)=REFLEV
1076    DO 1066 I=2,8
        IF (ACCDE(I)-DSA(I)) 1080,1085,1085
1080    COMP(I)=0.0
        GOTO 1066
1085    COMP(I)=REFLEV
1066    CONTINUE
C
C
```

```
C       ******* BEGIN DIGITAL CCD SHIFT REG. SIMULATIØN *******
C
      EFFIC=0.9999
      HFSMAG=2.71828182**(-2.0*(1.0-EFFIC)*(1.0-C0S(6.2832
     5*FSUBS/CKFRE0)))
      THERMI=0.000000001*2.71828182**((-1.11/0.00017)*((1.0
     6/(273.0+TEMP))-(1.0/298.0)))*(1000000/(CKFRE0*0.000001))
      D0 2010 I=1,8
      D0 2010 J=1,7
2010  DCCDE(I,9-J)=(DCCDE(I,8-J)*HFSMAG)+(DCCDE(I,9-J)-(
     7DCCDE(I,9-J)*HFSMAG))+THERMI
      D0 2012 I=1,8
2012  DCCDE(I,1)=C0MP(I)+(DCCDE(I,1)-(DCCDE(I,1)*HFSMAG))+THERMI
C
C
C       ******* BEGIN ANAL0G CCD SHIFT REG. SIMULATIØN *******
C
      D0 2014 I=1,7
2014  ACCDE(9-I)=(ACCDE(8-I)*HFSMAG)+(ACCDE(9-I)-(ACCDE(9-I)
     8*HFSMAG))+THERMI
      ACCDE(1)=ANIFCN(CP)+(ACCDE(1)-(ACCDE(1)*HFSMAG))+THERMI
C
C
C       ********* BEGIN 0UTPUT SIMULAT0R & LISTING *********
C
      D0 2020 I=1,8
2020  DI0DE(I)=(DCCDE(I,9-I)*HFSMAG)
      T0TALN=9.0
      D0 2030 I=1,8
      T0TALN=T0TALN-1.0
      HFSMAG=2.71828182**(-T0TALN*(1.0-EFFIC)*(1.0-C0S(6.2832
     9*FSUBS/CKFRE0)))
      IF (DI0DE(I)-(REFLEV*HFSMAG/2.0))2024,2024,2026
2024  0UTPUT(I)=R0
      G0T0 2030
2026  0UTPUT(I)=R1
2030  C0NTINUE
6543  F0RMAT(//)
      WRITE(6,6543)
8100  F0RMAT(3X,' CP(',I3,'  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
     6/\/\/\/\/\/\')
      WRITE(6,8100)CP
1221  WRITE(6,2035)0UTPUT(1),0UTPUT(2),0UTPUT(3),0UTPUT(4),
     90UTPUT(5),0UTPUT(6),0UTPUT(7),0UTPUT(8)
2035  F0RMAT(' CCD-VTF-A/D 0UTPUT [MSB FIRST] =  ',8A1)
2037  F0RMAT(' INTERNAL D/A 0UTPUTS [MSB D/A 0N LEFT] ARE:')
      WRITE(6,2037)
      WRITE(6,2036)DSA(1),DSA(2),DSA(3),DSA(4),DSA(5),DSA(6),
     8DSA(7),DSA(8)
2036  F0RMAT(8F7.4)
8333  F0RMAT(' THE F0LL0WING IS A LISTING 0F THE C0NTENTS 0F THE DIGITAL
     4 CCD SHFT REGS')
```

```
8334  FØRMAT(' (MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)')
      WRITE(6,8333)
      WRITE(6,8334)
      WRITE(6,8335)DCCDE(1,1),DCCDE(1,2),DCCDE(1,3),DCCDE(1,4),
     5DCCDE(1,5),DCCDE(1,6),DCCDE(1,7),DCCDE(1,8)
8335  FØRMAT(8F7.5)
      WRITE(6,8336)DCCDE(2,1),DCCDE(2,2),DCCDE(2,3),DCCDE(2,4),
     4DCCDE(2,5),DCCDE(2,6),DCCDE(2,7)
8336  FØRMAT(7F7.5)
      WRITE(6,8337)DCCDE(3,1),DCCDE(3,2),DCCDE(3,3),DCCDE(3,4),
     3DCCDE(3,5),DCCDE(3,6)
8337  FØRMAT(6F7.5)
      WRITE(6,8338)DCCDE(4,1),DCCDE(4,2),DCCDE(4,3),DCCDE(4,4),
     2DCCDE(4,5)
8338  FØRMAT(5F7.5)
      WRITE(6,8339)DCCDE(5,1),DCCDE(5,2),DCCDE(5,3),DCCDE(5,4)
8339  FØRMAT(4F7.5)
      WRITE(6,8400)DCCDE(6,1),DCCDE(6,2),DCCDE(6,3)
8400  FØRMAT(3F7.5)
      WRITE(6,8401)DCCDE(7,1),DCCDE(7,2)
8401  FØRMAT(2F7.5)
      WRITE(6,8402)DCCDE(8,1)
8402  FØRMAT(F7.5)
      WRITE(6,8440)
8440  FØRMAT(' THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG
     4CCD SHIFT REGS  (TØP ELEMENT FIRST)')
      WRITE(6,8441)ACCDE(1),ACCDE(2),ACCDE(3),ACCDE(4),
     4ACCDE(5),ACCDE(6),ACCDE(7),ACCDE(8)
8441  FØRMAT(8F7.5)
C
C
4444  CØNTINUE
      STØP
7777  END
SCAN:237
```

APPENDIX IV

SAMPLE RUN

```
*****************************************************
*                                                   *
*          CCD-VTF-A/D SIMULATIØN PRØGRAM           *
*                                                   *
*****************************************************
```

THE FØLLØWING PARAMETERS HAVE BEEN SELECTED:

NØ. ØF CLØCK TIMES TØ BE DISPLAYED: 22
CLØCK FREQUENCY: 100.0000 MHZ
LØGIC 1 REFERENCE LEVEL: .2500 VØLTS
SUBSTRATE TEMPERATURE: 25.000 DEG. CELCIUS

THE FØLLØWING 22 PAIRS ØF NUMBERS REPRESENT THE
SAMPLED ANALØG INPUTS TØ THE CØNVERTER AND THEIR
CØRRESPØNDING IDEAL BINARY VALUES:

.000000	.....	0.0
.000000	.....	0.0
.198473	.....	0.00110010110011111100100
.243682	.....	0.00111110011
.243882	.....	0.00111110011
.198473	.....	0.00110010110011111100100
.125000	.....	0.0010
.051527	.....	0.00001101001
.006118	.....	0.00000001100100001111 0
.006118	.....	0.00000001100100001111 0
.051527	.....	0.00001101001
.125000	.....	0.0010
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0
.000000	.....	0.0

```
   CP( 1 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT [MSB FIRST] =  00000000
INTERNAL D/A ØUTPUTS [MSB D/A ØN LEFT] ARE:
 .1250  .0625  .0313  .0156  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
[MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST]
.00001 .00001 .00001 .00001 .00001 .00001 .00001 .00001
.00001 .00001 .00001 .00001 .00001 .00001 .00001
.00001 .00001 .00001 .00001 .00001 .00001
.00001 .00001 .00001 .00001 .00001
.00001 .00001 .00001 .00001
.00001 .00001 .00001
.00001 .00001
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 [TØP ELEMENT FIRST]
.00001 .00001 .00001 .00001 .00001 .00001 .00001 .00001

   CP( 2 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT [MSB FIRST] =  00000000
INTERNAL D/A ØUTPUTS [MSB D/A ØN LEFT] ARE:
 .1250  .0625  .0313  .0156  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
[MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST]
.00001 .00002 .00002 .00002 .00002 .00002 .00002 .00002
.00001 .00002 .00002 .00002 .00002 .00002 .00002
.00001 .00002 .00002 .00002 .00002 .00002
.00001 .00002 .00002 .00002 .00002
.00001 .00002 .00002 .00002
.00001 .00002 .00002
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 [TØP ELEMENT FIRST]
.00001 .00002 .00002 .00002 .00002 .00002 .00002 .00002

   CP( 3 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT [MSB FIRST] =  00000000
INTERNAL D/A ØUTPUTS [MSB D/A ØN LEFT] ARE:
 .1250  .0625  .0313  .0156  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
[MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST]
.00001 .00002 .00003 .00003 .00003 .00003 .00003 .00003
.00001 .00002 .00003 .00003 .00003 .00003 .00003
.00001 .00002 .00003 .00003 .00003 .00003
.00001 .00002 .00003 .00003 .00003
.00001 .00002 .00003 .00003
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 [TØP ELEMENT FIRST]
.19848 .00002 .00003 .00003 .00003 .00003 .00003 .00003
```

```
   CP( 4 )  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
 CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
 INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
  .1250  .0625  .0313  .0156  .0078  .0039  .0020  .0010
 THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
 (MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
 .25001 .00002 .00003 .00004 .00004 .00004 .00004 .00004
 .00001 .00002 .00003 .00004 .00004 .00004 .00004
 .00001 .00002 .00003 .00004 .00004 .00004
 .00001 .00002 .00003 .00004 .00004
 .00001 .00002 .00003 .00004
 .00001 .00002 .00003
 .00001 .00002
 .00001
 THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
  (TØP ELEMENT FIRST)
 .24397 .19841 .00003 .00004 .00004 .00004 .00004 .00004
```

```
   CP( 5 )  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .1875  .0313  .0156  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.25011 .24992 .00003 .00004 .00005 .00005 .00005 .00005
.25001 .00002 .00003 .00004 .00005 .00005 .00005
.00001 .00002 .00003 .00004 .00005 .00005
.00001 .00002 .00003 .00004 .00005
.00001 .00002 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.24399 .24396 .19834 .00004 .00005 .00005 .00005 .00005
```

```
   CP( 6 )  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .1876  .2187  .0156  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.25011 .25012 .24983 .00004 .00005 .00006 .00006 .00006
.25011 .24992 .00003 .00004 .00005 .00006 .00006
.00001 .00002 .00003 .00004 .00005 .00006
.00001 .00002 .00003 .00004 .00005
.00001 .00002 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.19858 .24400 .24395 .19827 .00005 .00006 .00006 .00006
```

```
   CP( 7 )  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .1876  .2188  .2030  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.25011 .25012 .25013 .24974 .00005 .00006 .00007 .00007
.25011 .25012 .24983 .00004 .00005 .00006 .00007
.25001 .00002 .00003 .00004 .00005 .00006
.00001 .00002 .00003 .00004 .00005
.00001 .00002 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.12509 .19861 .24401 .24395 .19821 .00006 .00007 .00007


   CP( 8 )  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .1876  .2188  .2345  .1951  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.25011 .25012 .25013 .25014 .24965 .00006 .00007 .00008
.25011 .25012 .25013 .24974 .00005 .00006 .00007
.25011 .24992 .00003 .00004 .00005 .00006
.25001 .00002 .00003 .00004 .00005
.25001 .00002 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.05159 .12513 .19864 .24402 .24394 .19814 .00007 .00008


   CP( 9 )  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .1876  .2188  .2345  .2423  .1990  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00011 .25012 .25013 .25014 .25015 .24956 .00007 .00008
.00011 .25012 .25013 .25014 .24965 .00006 .00007
.00011 .25012 .24983 .00004 .00005 .00006
.25011 .24992 .00003 .00004 .00005
.25011 .24992 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00615 .05163 .12517 .19867 .24403 .24393 .19807 .00008
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   CP( 10 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0626  .1563  .2032  .2423  .2462  .1970  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00022 .25013 .25014 .25015 .25016 .24947 .00008
.00001 .00022 .25013 .25014 .25015 .24956 .00007
.00001 .00022 .25013 .24974 .00005 .00006
.00011 .25012 .24983 .00004 .00005
.25011 .25012 .24983 .00004
.00001 .00002 .00003
.25001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00613 .00618 .05167 .12521 .19869 .24404 .24392 .19800


   CP( 11 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  11001011
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0314  .1407  .1954  .2462  .2442  .1979
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00002 .00033 .25014 .25015 .25016 .25017 .24938
.00001 .00002 .00033 .25014 .25015 .25016 .24947
.25001 .00002 .00033 .25014 .24965 .00006
.00001 .00022 .25013 .24974 .00005
.25011 .25012 .25013 .24974
.00001 .00002 .00003
.00011 .24992
.25001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.05154 .00614 .00621 .05171 .12525 .19672 .24405 .24391


   CP( 12 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  11111001
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0313  .0470  .1330  .1994  .2443  .2432
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00002 .00003 .00044 .25015 .25016 .25017 .25018
.00001 .00002 .00003 .00044 .25015 .25016 .25017
.00011 .24992 .00003 .00044 .25015 .24956
.25001 .00002 .00033 .25014 .24965
.00011 .25012 .25013 .25014
.00001 .00002 .00003
.00001 .00022
.25011
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.12503 .05153 .00615 .00623 .05174 .12529 .19875 .24406
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   CP( 13 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  11111001
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0313  .0157  .0549  .1291  .1975  .2433
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.25001 .00002 .00003 .00004 .00055 .25016 .25017 .25018
.00001 .00002 .00003 .00004 .00055 .25016 .25017
.00001 .00022 .24983 .00004 .00055 .25016
.00011 .24992 .00003 .00044 .25015
.00001 .00022 .25013 .25014
.00001 .00002 .00003
.25001 .00002
.25011
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00006 .12501 .05152 .00616 .00626 .05178 .12533 .19878


   CP( 14 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  11001011
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .1875  .0313  .0156  .0079  .0510  .1272  .1985
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00011 .24992 .00003 .00004 .00005 .00066 .25017 .25018
.00001 .00002 .00003 .00004 .00005 .00066 .25017
.25001 .00002 .00033 .24974 .00005 .00066
.00001 .00022 .24983 .00004 .00055
.00001 .00002 .00033 .25014
.25001 .00002 .00003
.00011 .24992
.25011
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00001 .00012 .12499 .05152 .00617 .00629 .05182 .12537


   CP( 15 )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  10000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0626  .1562  .0469  .0078  .0040  .0530  .1262
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00022 .24983 .00004 .00005 .00006 .00077 .25018
.00001 .00002 .00003 .00004 .00005 .00006 .00077
.00011 .24992 .00003 .00044 .24965 .00006
.25001 .00002 .00033 .24974 .00005
.00001 .00002 .00003 .00044
.25011 .24992 .00003
.00001 .00022
.00011
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00001 .00002 .00018 .12497 .05151 .00618 .00632 .05186
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   CP( 16  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT [MSB FIRST] =  00110100
INTERNAL D/A ØUTPUTS [MSB D/A ØN LEFT] ARE:
 .1250  .0625  .0314  .1406  .0547  .0039  .0060  .0521
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
[MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST]
.00001 .00002 .00033 .24974 .00005 .00006 .00007 .00068
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00022 .24983 .00004 .00055 .24956
.00011 .24992 .00003 .00044 .24965
.00001 .00002 .00003 .00004
.25011 .25012 .24983
.25001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 [TØP ELEMENT FIRST]
.00001 .00002 .00003 .00024 .12495 .05150 .00619 .00635
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   CP( 17  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT [MSB FIRST] =  00000110
INTERNAL D/A ØUTPUTS [MSB D/A ØN LEFT] ARE:
 .1250  .0625  .0313  .0158  .1327  .0508  .0059  .0070
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
[MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST]
.00001 .00002 .00003 .00044 .24965 .00006 .00007 .00008
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00002 .00033 .24974 .00005 .00066
.00001 .00022 .24983 .00004 .00055
.00001 .00002 .00003 .00004
.25011 .25012 .25013
.25011 .24992
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 [TØP ELEMENT FIRST]
.00001 .00002 .00003 .00004 .00030 .12493 .05149 .00620
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   CP( 18  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT [MSB FIRST] =  00000110
INTERNAL D/A ØUTPUTS [MSB D/A ØN LEFT] ARE:
 .1250  .0625  .0313  .0156  .0080  .1288  .0527  .0069
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
[MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST]
.00001 .00002 .00003 .00004 .00055 .24956 .00007 .00008
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00002 .00003 .00044 .24965 .00006
.00001 .00002 .00033 .24974 .00005
.00001 .00002 .00003 .00004
.00011 .25012 .25013
.00011 .25012
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 [TØP ELEMENT FIRST]
.00001 .00002 .00003 .00004 .00005 .00036 .12491 .05148
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   CP( 19  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00110100
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0313  .0156  .0078  .0042  .1268  .0518
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00066 .24947 .00008
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00002 .00003 .00004 .00055 .24956
.00001 .00002 .00003 .00044 .24965
.00001 .00002 .00003 .00004
.00001 .00022 .25013
.00001 .00022
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00042 .12489


   CP( 20  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  10000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0313  .0156  .0078  .0039  .0023  .1258
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00077 .24938
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00002 .00003 .00004 .00005 .00066
.00001 .00002 .00003 .00004 .00055
.00001 .00002 .00003 .00004
.00001 .00002 .00033
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00007 .00048


   CP( 21  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0313  .0156  .0078  .0039  .0020  .0014
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00007 .00088
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00002 .00003 .00004 .00005 .00006
.00001 .00002 .00003 .00004 .00005
.00001 .00002 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00007 .00008
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   CP( 22  )   \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
CCD-VTF-A/D ØUTPUT (MSB FIRST) =  00000000
INTERNAL D/A ØUTPUTS (MSB D/A ØN LEFT) ARE:
 .1250  .0625  .0313  .0156  .0078  .0039  .0020  .0010
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE DIGITAL CCD SHFT REGS
(MSB SHIFT REG. FIRST / LEFTMØST ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00007 .00008
.00001 .00002 .00003 .00004 .00005 .00006 .00007
.00001 .00002 .00003 .00004 .00005 .00006
.00001 .00002 .00003 .00004 .00005
.00001 .00002 .00003 .00004
.00001 .00002 .00003
.00001 .00002
.00001
THE FØLLØWING IS A LISTING ØF THE CØNTENTS ØF THE ANALØG CCD SHIFT REGS
 (TØP ELEMENT FIRST)
.00001 .00002 .00003 .00004 .00005 .00006 .00007 .00008

NØRMAL EXIT.  EXECUTIØN TIME:          1310 MLSEC.
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